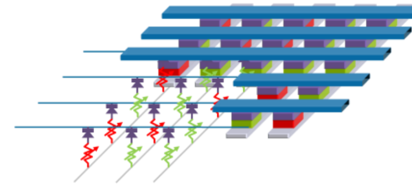
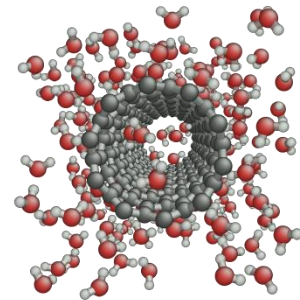
NON-VOLATILE MEMORY DEVICES: FROM SILICON TO ORGANIC MATERIALS





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Lecture for the course «Tecnologie e dispositivi elettronici avanzati»

November, 2015

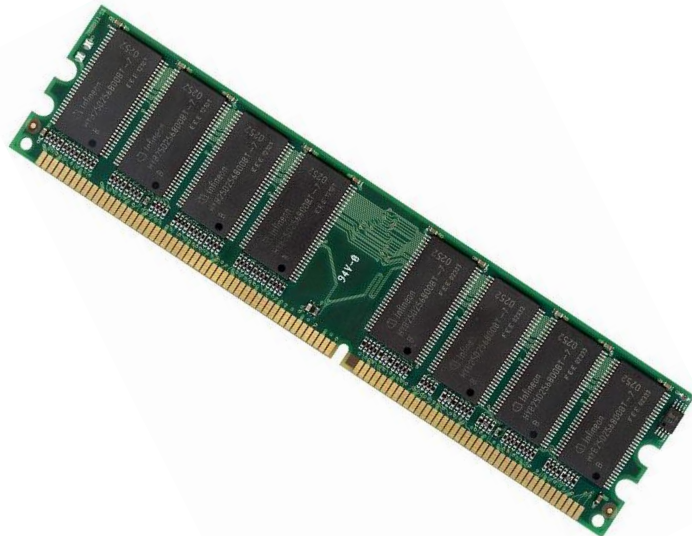
Outline

- Introduction: memory concept and classification
- Conventional memory technologies
- Emerging memory technologies: from inorganic to organic electronics
- Potential and challenges of organic memory devices
- Organic memory structures
- Organic transistor-type memories
  - Floating gate
  - Charge trapping
  - Ferroelectric

What is an electronic memory?

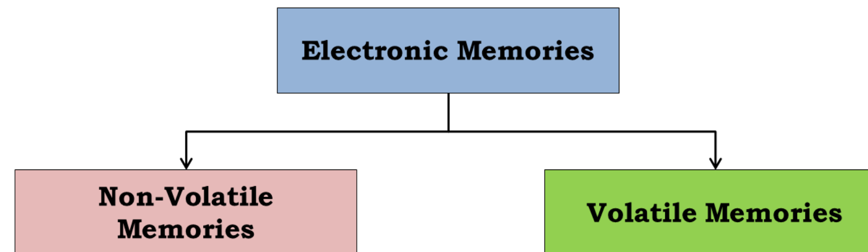
An electronic memory is a component, device or recording medium used to store data for retrieval on a termporary or permanent basis for use in a computer or other electronic devices

Electronic

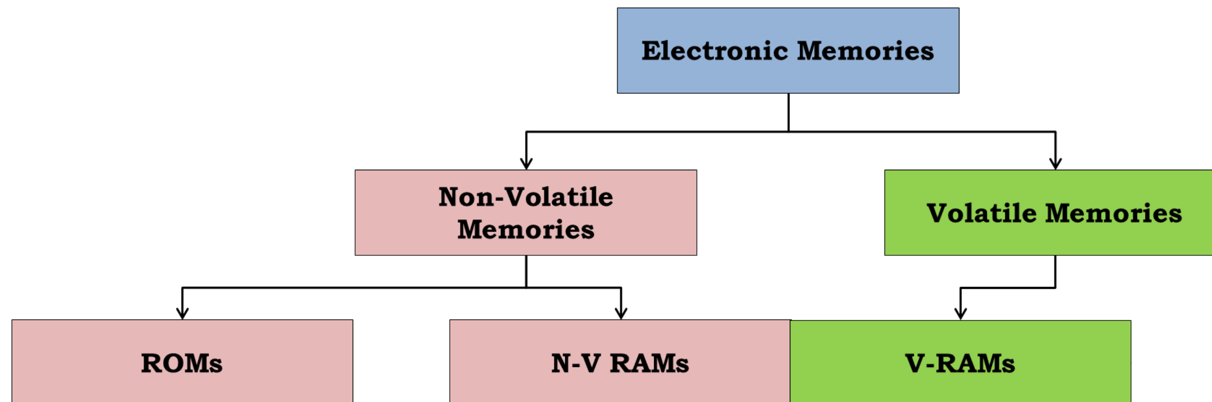


Mechanical (CD, DVD, Hard disk)

Classification of electronic memories



Classification of electronic memories



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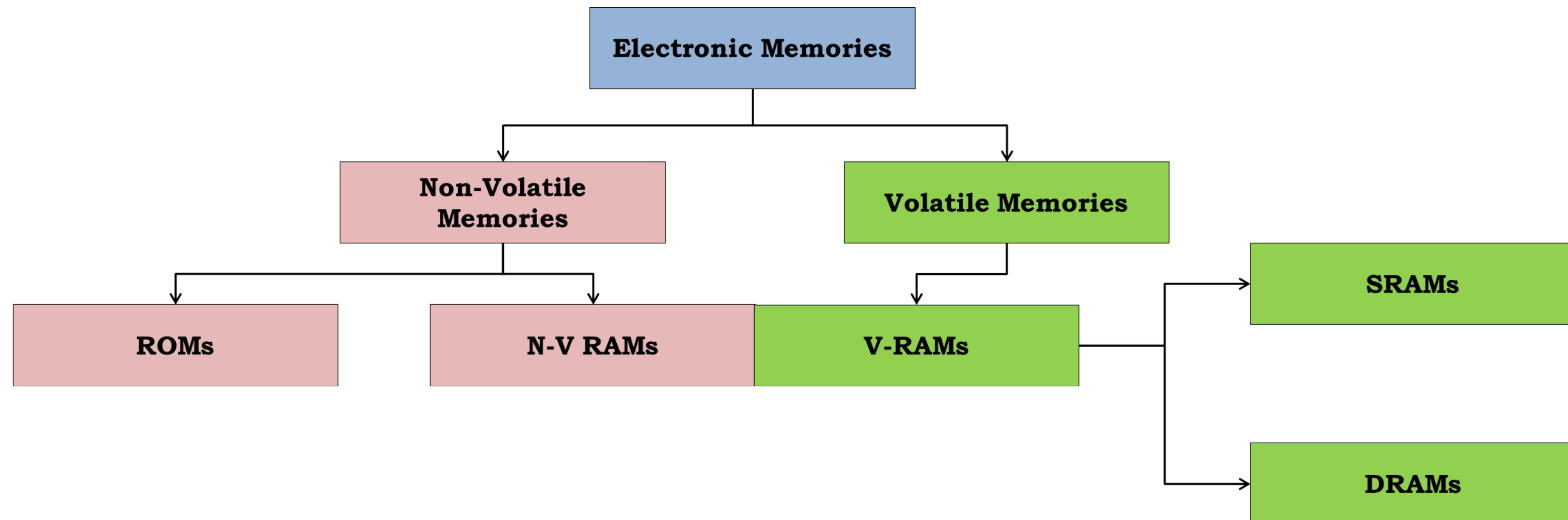
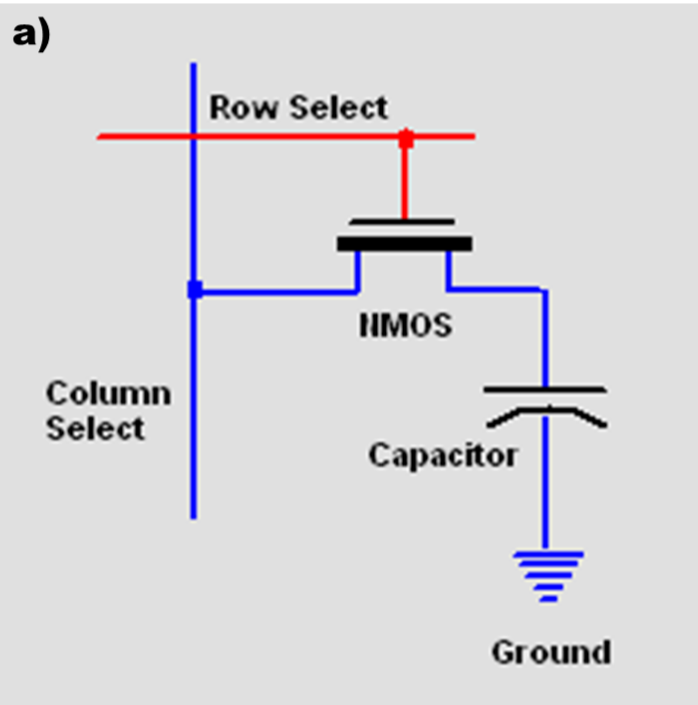
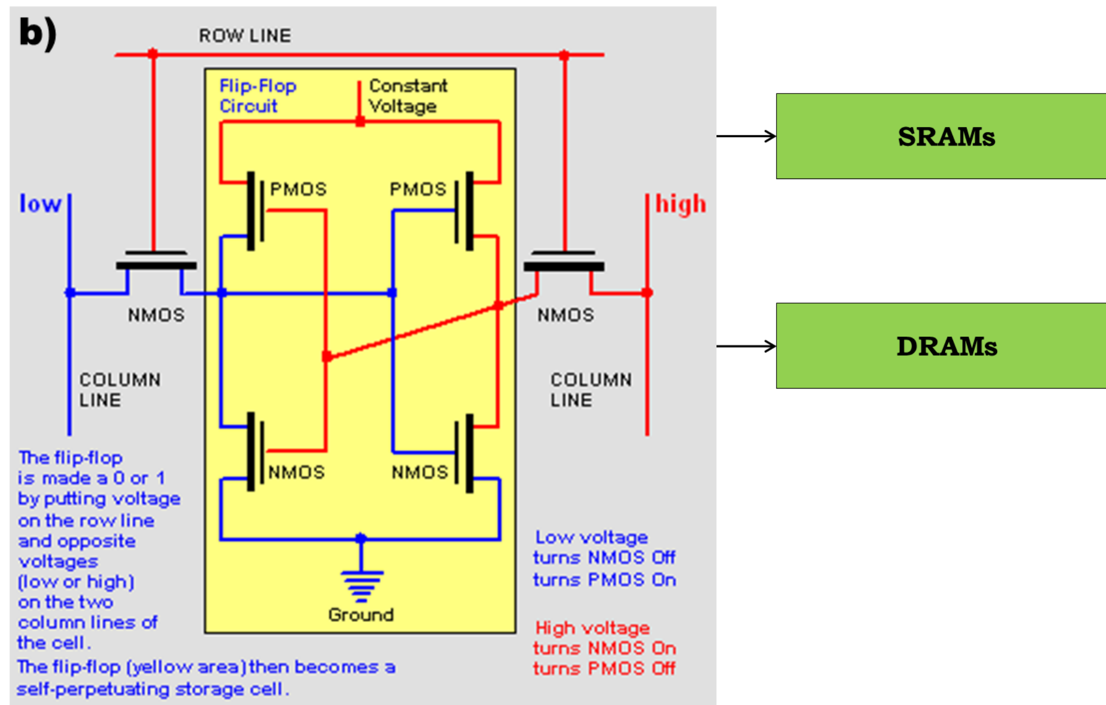


Classification of electronic memories

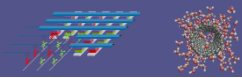
Electronic Memories



DRAM: Dinamic RAM



SRAM: Static RAM

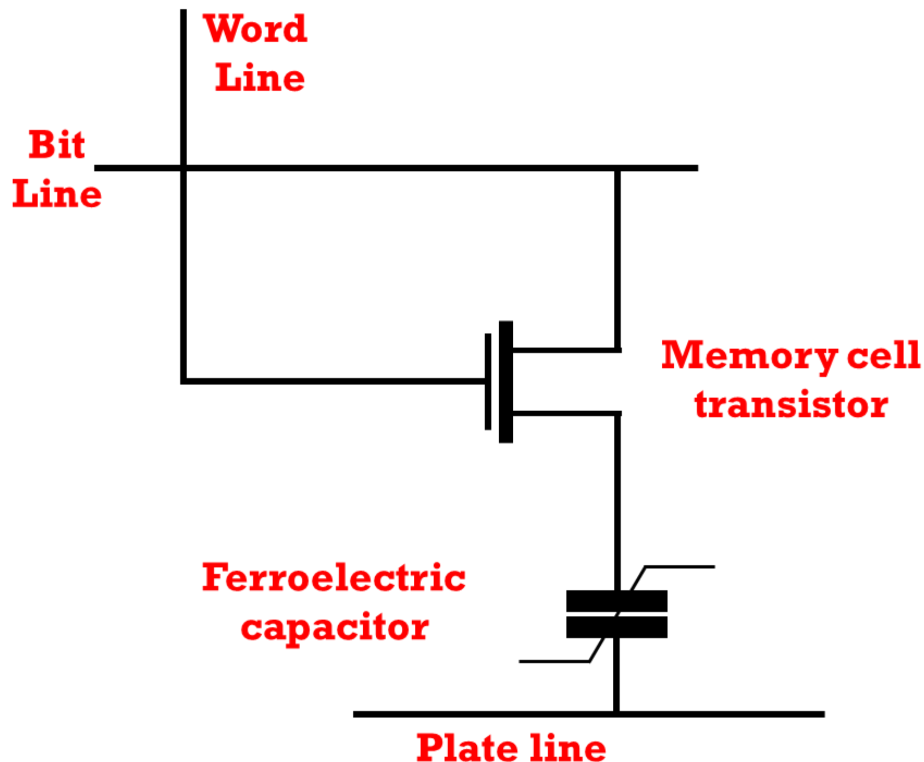


Classification of electronic memories

Electronic Memories
- Non-Volatile Memories
  - ROMs
  - N-V RAMs
    - FRAM
    - MRAM
    - PRAM
    - RRAM
- Volatile Memories
  - V-RAMs
    - SRAMs
    - DRAMs

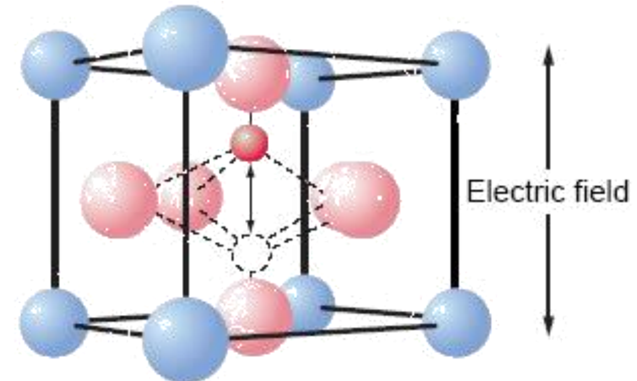
Classification of electronic memories

Ferroelectric RAM (FRAM)



What are ferroelectric materials??

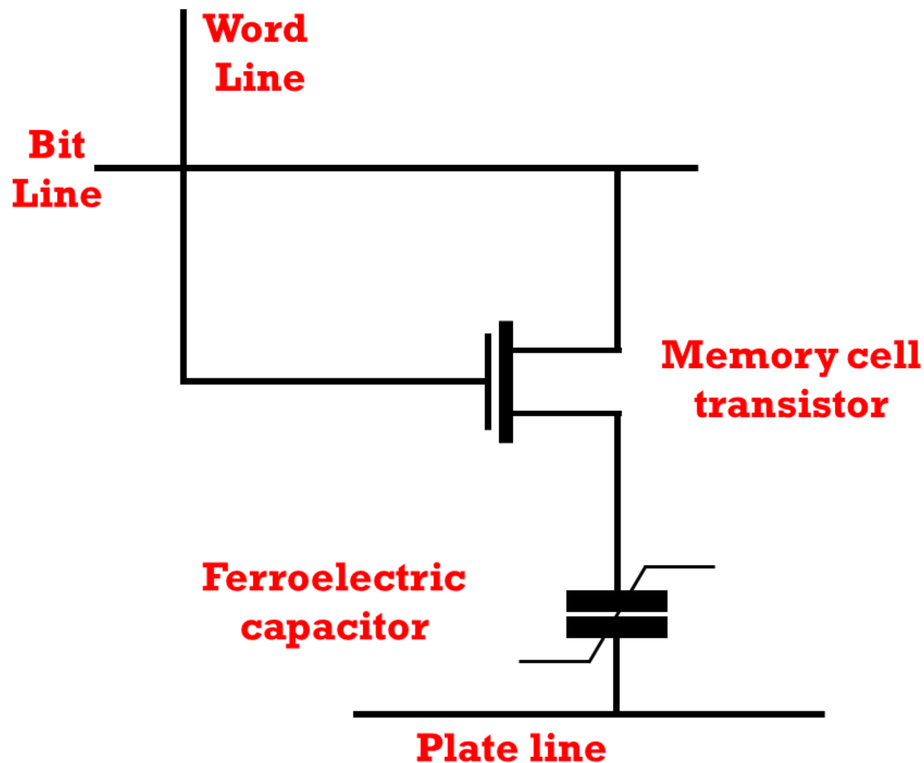
Materials composed of crystals in which the structural units are tiny electric dipoles

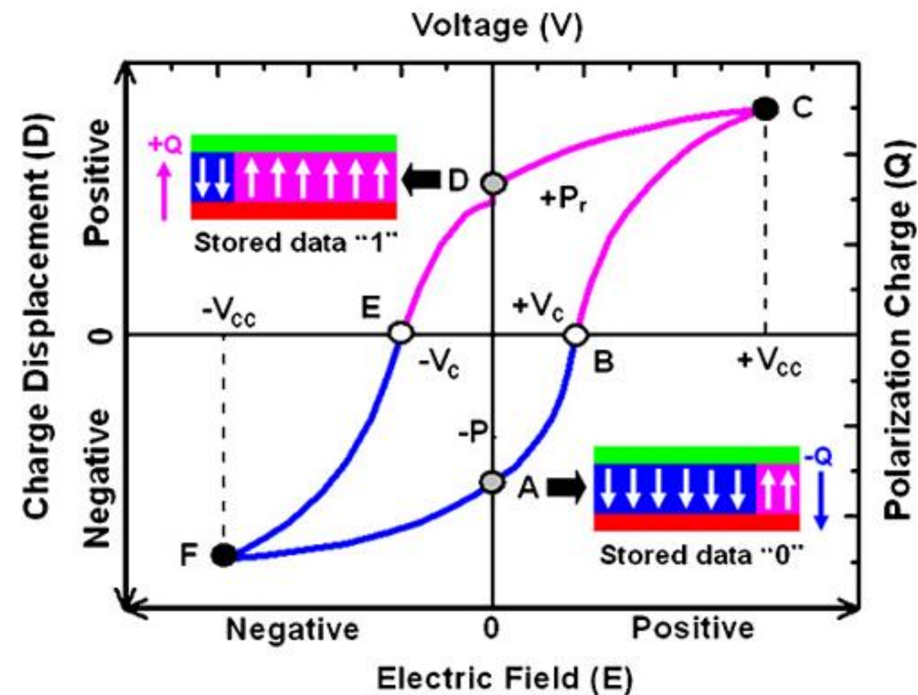


- Use electric field and ferroelectric effects to store data
- Exploit a ferroelectric capacitor
- Introduce in the late 1980s

Classification of electronic memories

Ferroelectric RAM (FRAM)





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Classification of electronic memories

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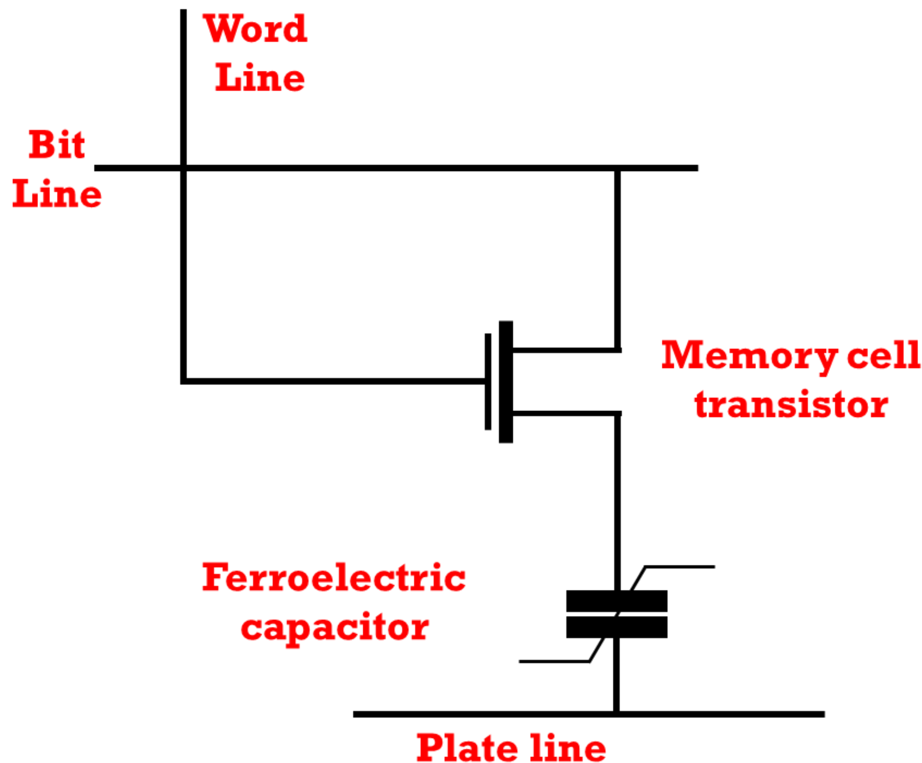


Advantages:

- Low power consumption
- Fast write speed
- Good cyclability

- Use electric field and ferroelectric effects to store data
- Exploit a ferroelectric capacitor
- Introduce in the late 1980s

Classification of electronic memories

Electronic Memories

Non-Volatile Memories

Volatile Memories

ROMs

N-V RAMs

V-RAMs

SRAMs

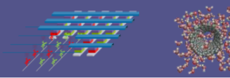
DRAMs

FRAM

MRAM

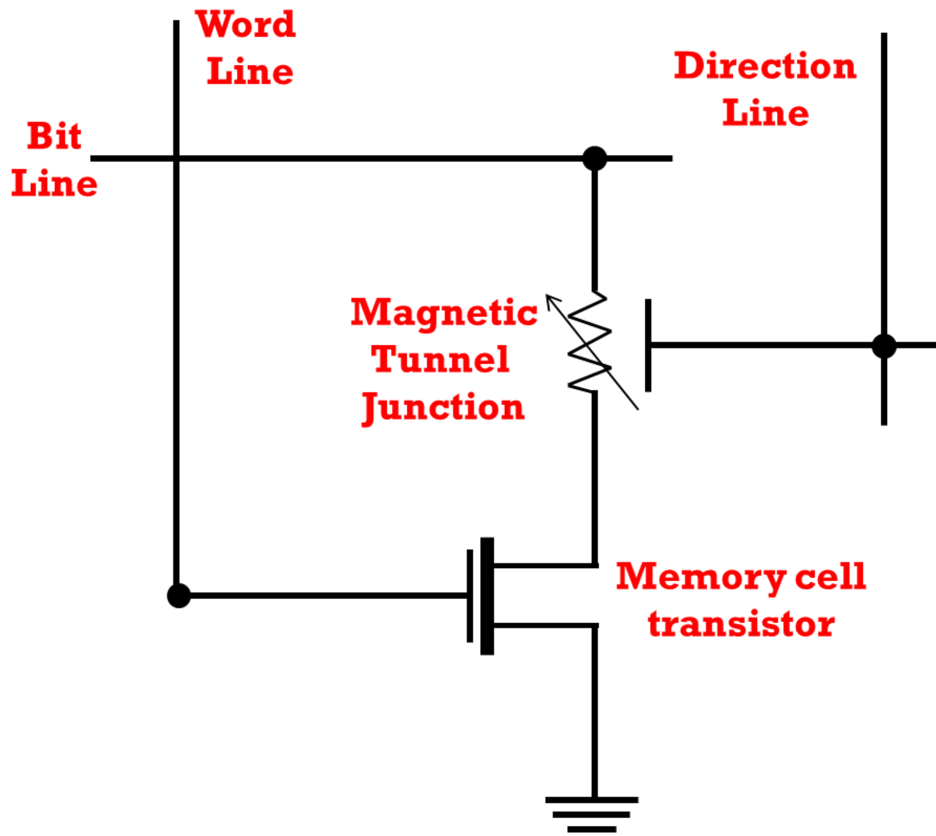
PRAM

RRAM



Classification of electronic memories

Magnetic RAM (MRAM)



- Data is not stored as electric charge or current flow, but by magnetic storage element
- Basic cell: Magnetic Tunnel Junction (MTJ)

Advantages:

- **Lower power consumption than DRAM**
- **Density similar to DRAM**
- **Much faster than DRAM**
- **Suffer no degradetion over time**

Classification of electronic memories

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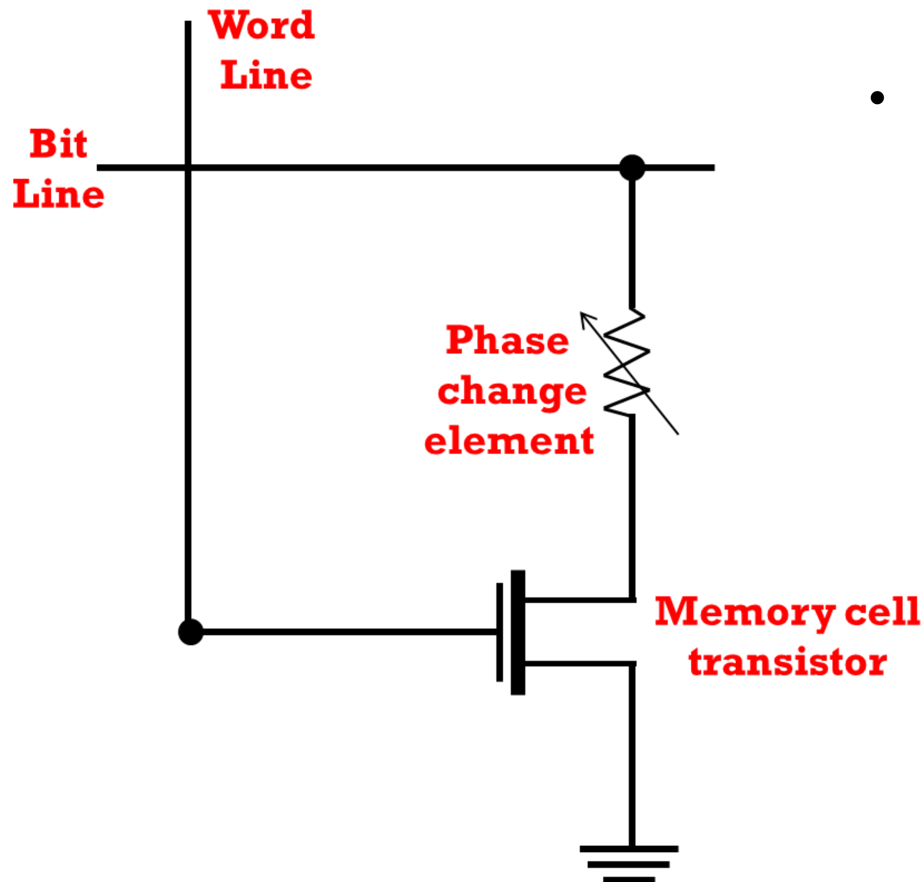
  - Volatile Memories
    - V-RAMs
      - SRAMs
      - DRAMs

Classification of electronic memories

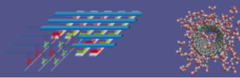
Phase-change RAM (PRAM)



- Exploit the unique property of phase-change materials (chalcogenides): reversible phase transition between amorphous (logic 0) and crystalline phases (logic 1)

Advantages:

- **Inherent scalability**
- **Switching time**



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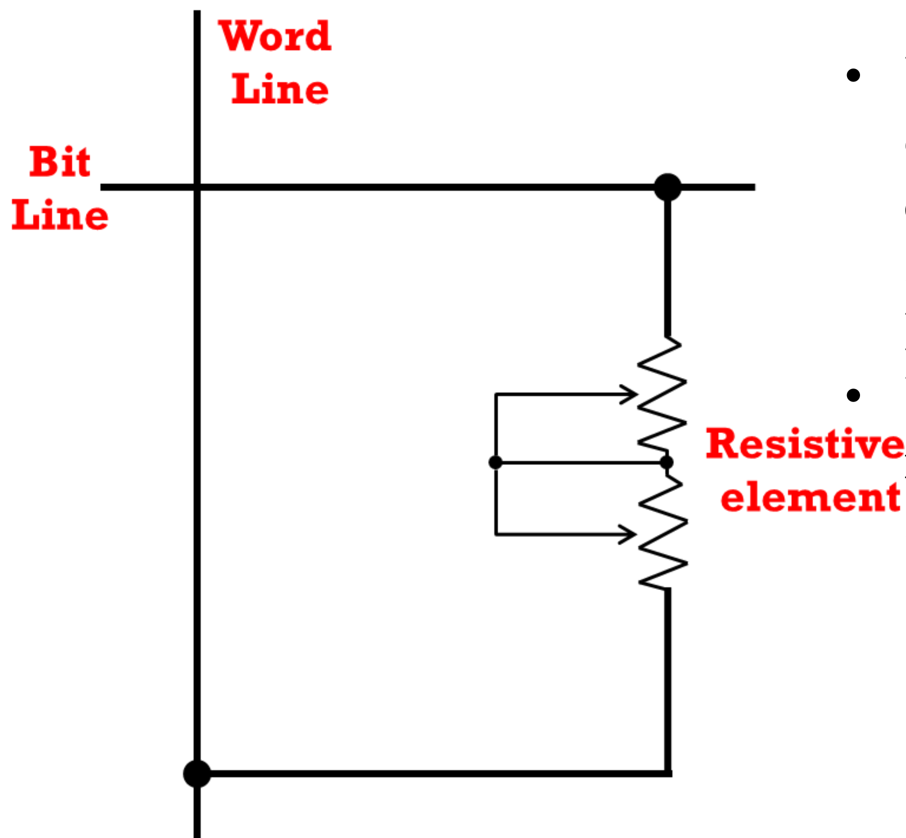
Classification of electronic memories

Resistive RAM (RRAM)



- Each cell consist of a top and a bottom electrode sandwiching a resistive layer, characterized by two resistance states: an high resistance state (HRS) and a low resistance state (LRS)
- By applying a voltage to the cell, resistive switching between the HRS and the LRS can be achieved

Advantages:

- **Simple and small structure**
- **No access transistors**
- **Integration in cross bar arrays**

Classification of electronic memories

Electronic Memories

Non-Volatile Memories

Volatile Memories

ROMs

N-V RAMs

V-RAMs

SRAMs

DRAMs

WORM

EPROM

FRAM

MRAM

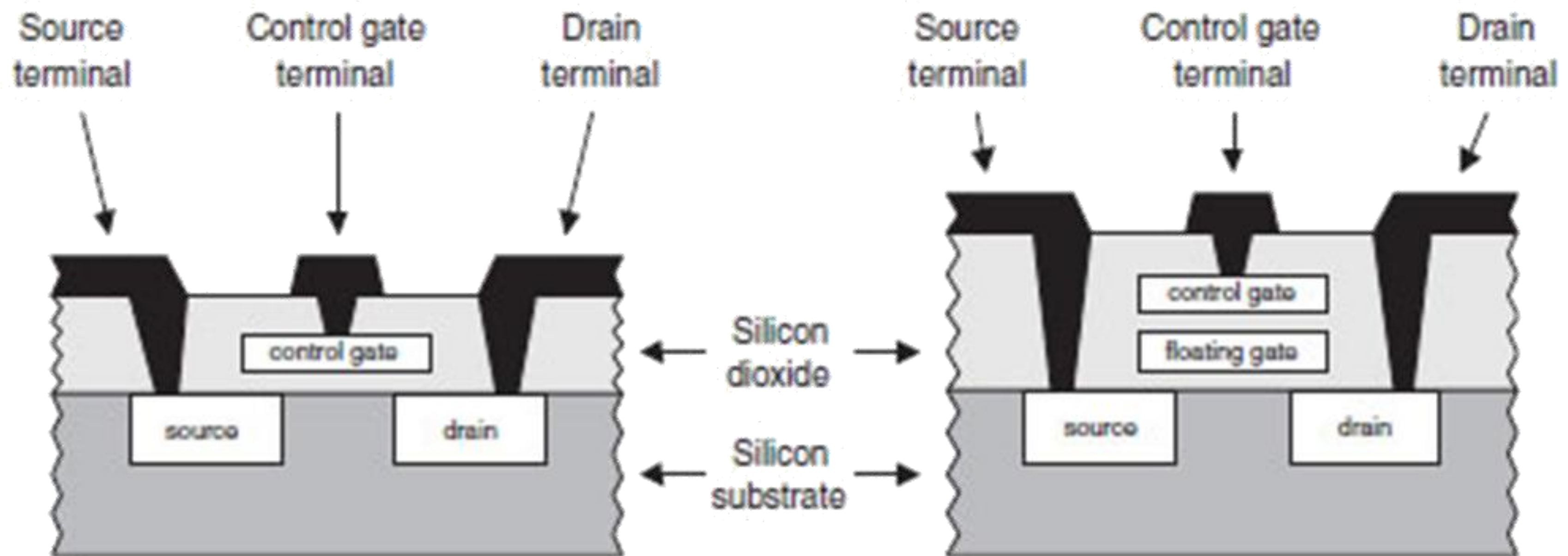
PRAM

RRAM

Classification of electronic memories

Classification of electronic memories

UVEPROM

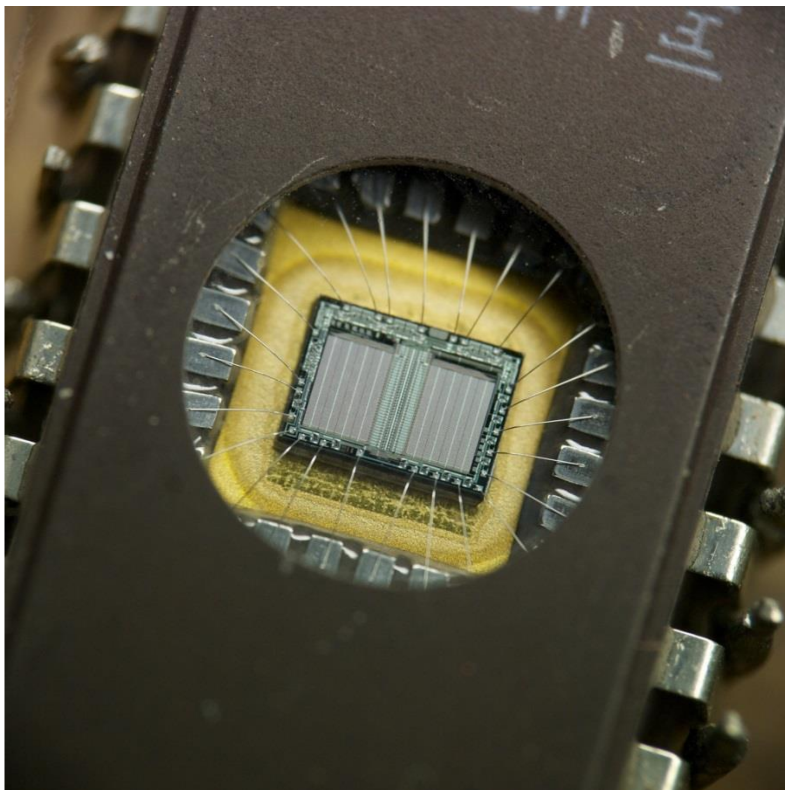


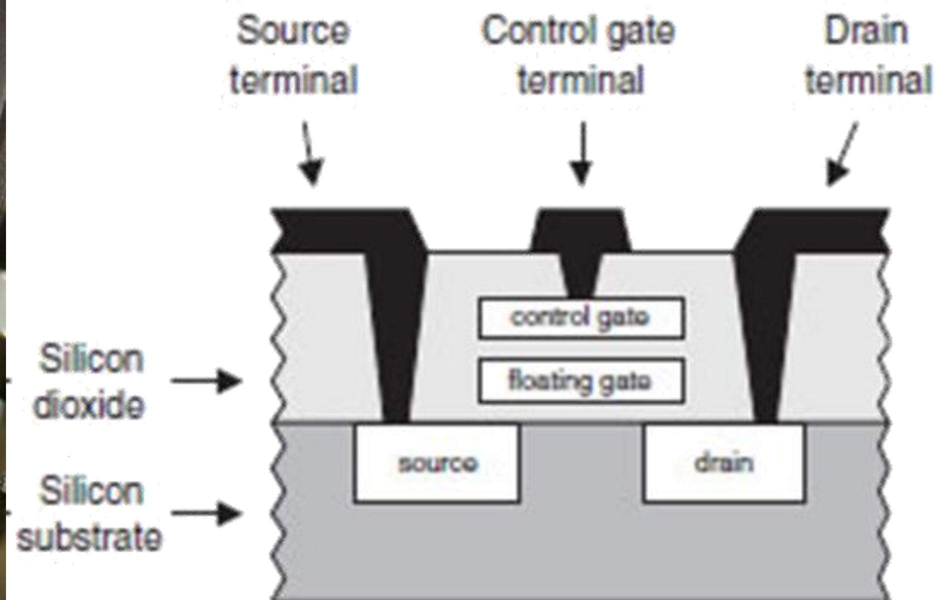
a) Standard MOS transistor

b) UVEPROM transistor

Classification of electronic memories

UVEPROM

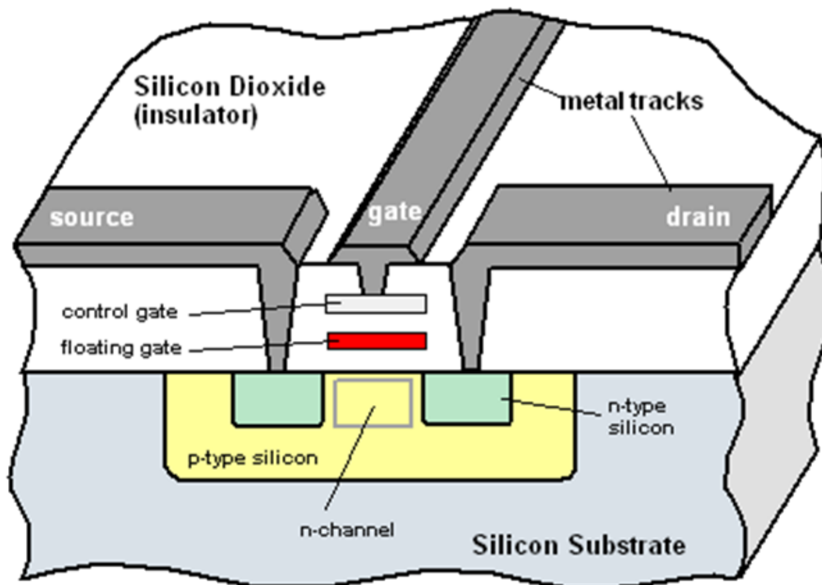


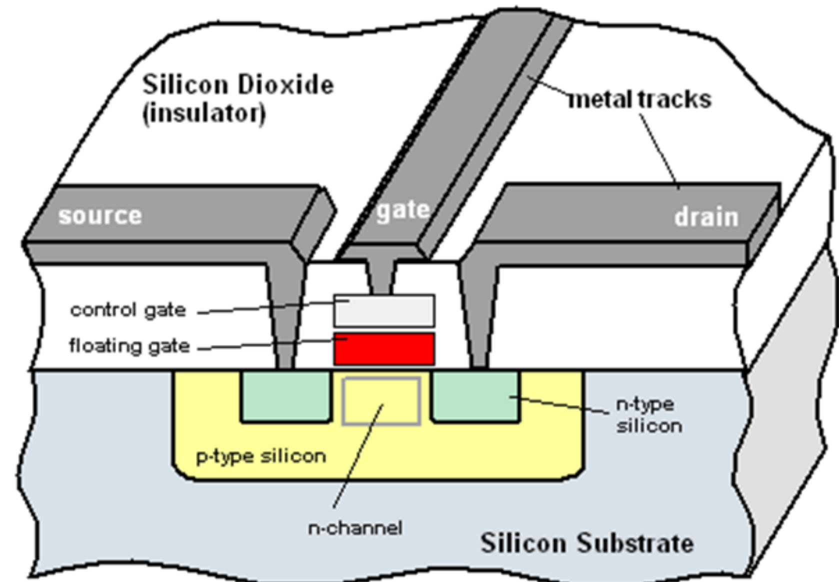


b) UVEPROM transistor

Classification of electronic memories

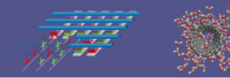
EEPROM



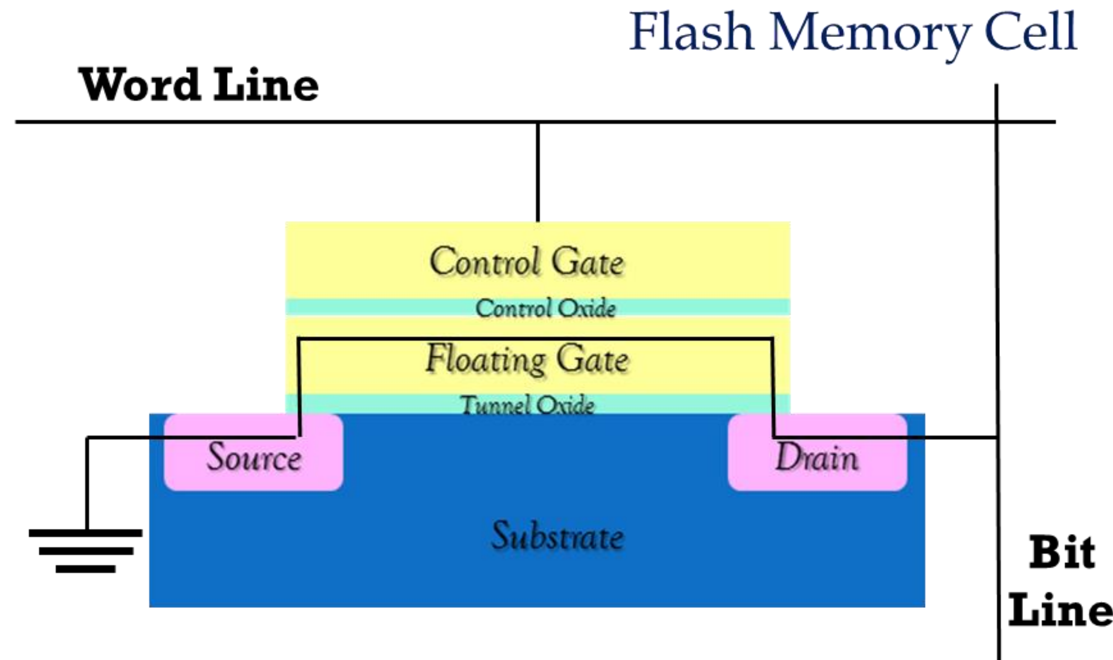


Classification of electronic memories

- Electronic Memories
  - Non-Volatile Memories
    - ROMs
      - WORM
      - EPROM
        - UVEPROM
        - EEPROM
          - FLASH
    - N-V RAMs
      - FRAM
      - MRAM
      - PRAM
      - RRAM
  - Volatile Memories
    - V-RAMs
      - SRAMs
      - DRAMs



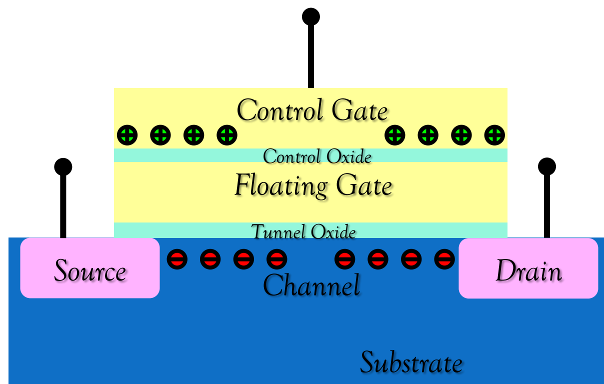
Flash Memories



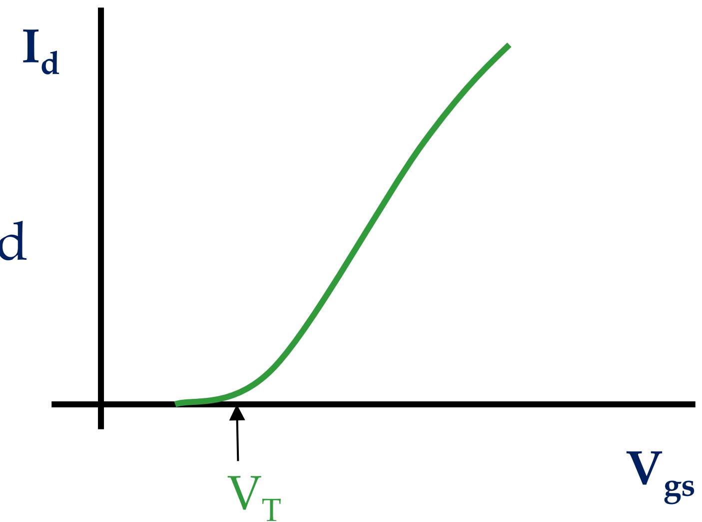
A Flash cell is basically a single floating-gate MOS transistor, i.e., a transistor with a gate completely surrounded by a insulating layer, the floating gate, and electrically governed by a capacitively coupled control gate.

Flash Memories: working principle

Writing process



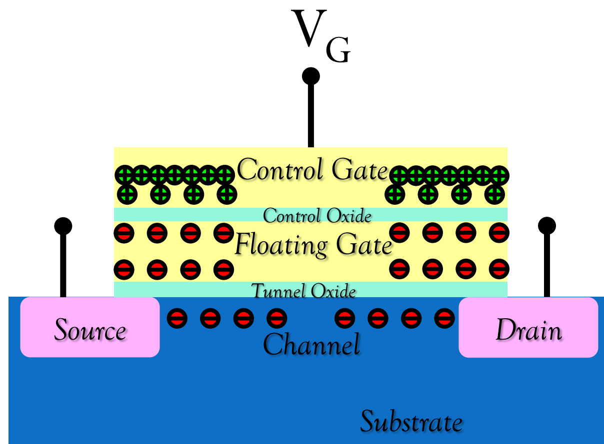
Unprogrammed



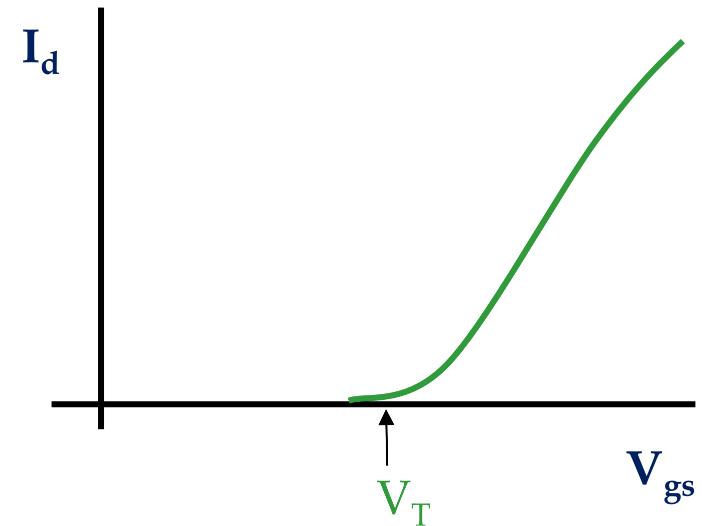
The application of voltage pulses to the *control gate* allows electrons from the *channel* to cross the *tunnel oxide* and charge the *floating gate* (modifying the *threshold voltage* V_t). Thus, the electrostatic potential of the floating gate screens the electrons of the channel, and the current between *source* and *drain* is substantially reduced.

Flash Memories: working principle

Writing process



Programmed



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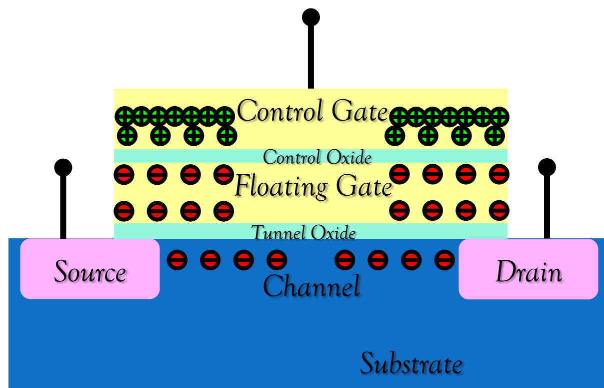
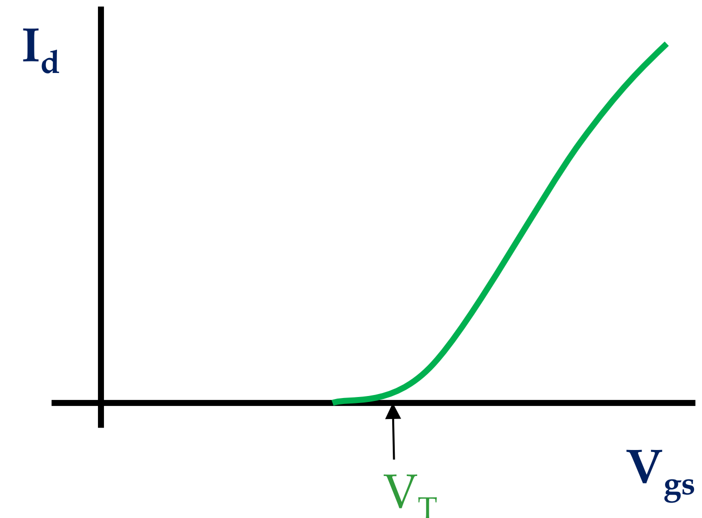
Flash Memories: working principle

Erase process



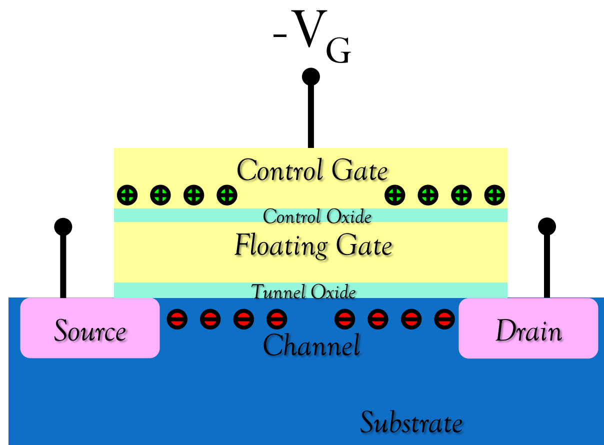
Programmed



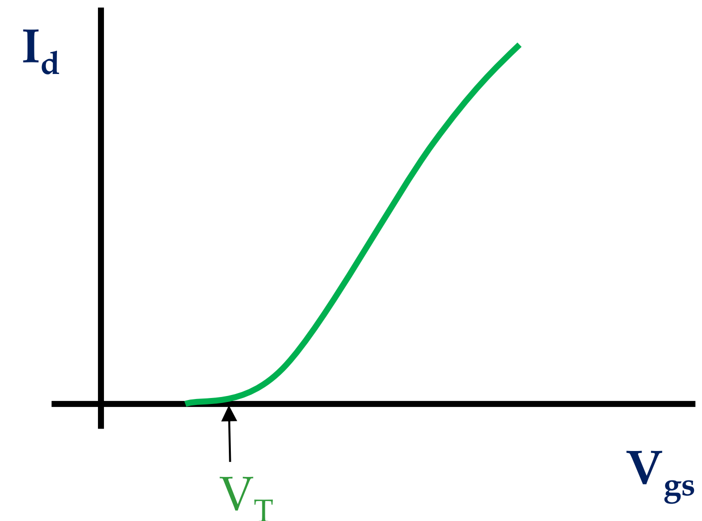
To remove the electrons from the floating gate, an opposite polarity voltage pulse is applied, which brings them back to the channel through the tunnel oxide. In this case, we observe that the source–drain current increases again.

Flash Memories: working principle

Erase process



Deleted



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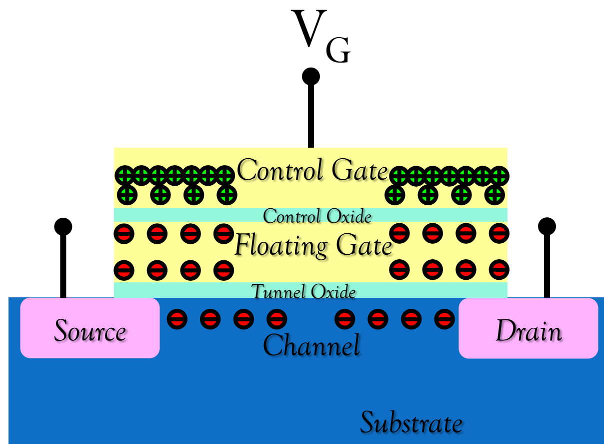
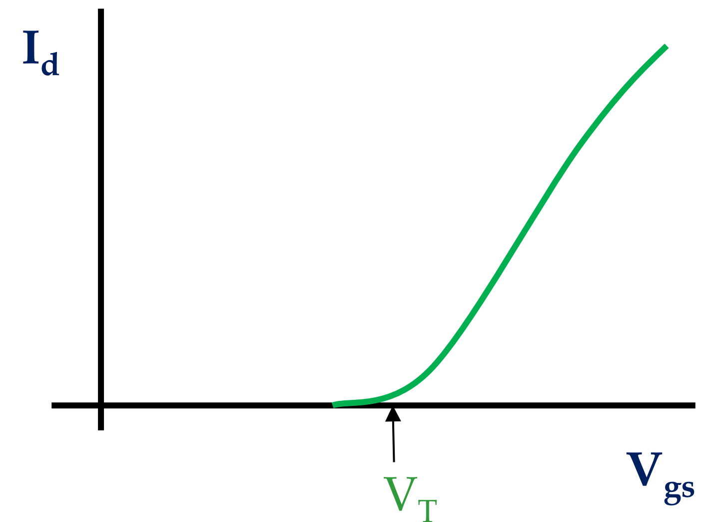
Flash Memories: working principle

Reading process



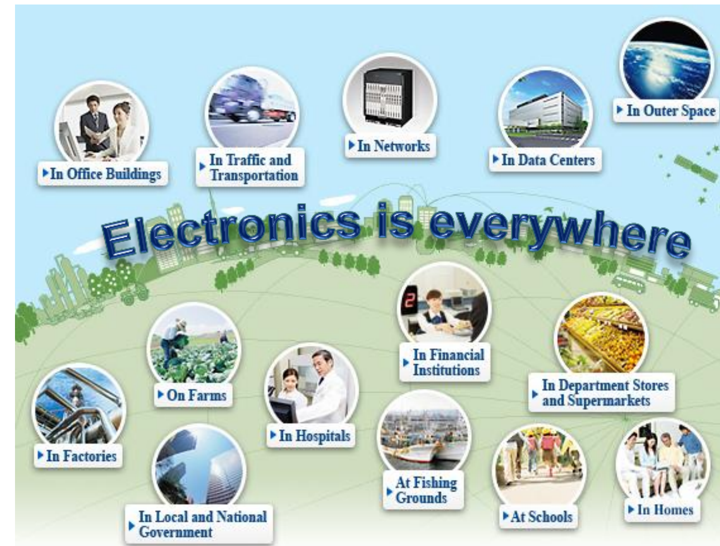
Programmed



The reading operation is performed evaluating the threshold voltage of the floating gate through the measurement of the drain current at a gate voltage that will not disturb the writing and erasing states of the device.

Conventional memory techonologies

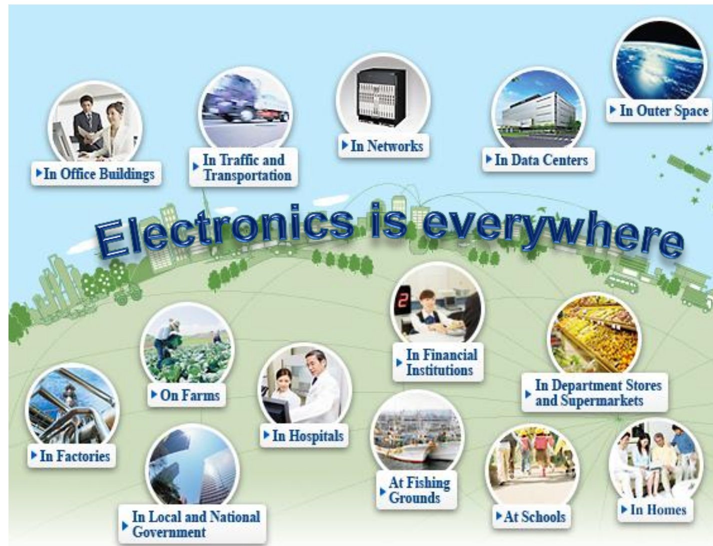
Conventional memory techonologies



Continuos flow of:
- **Faster**
- **Cheaper**
- **Smaller**

high-technology products

Conventional memory techonologies



Continuos flow of:

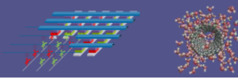
- Faster
- Cheaper
- Smaller

high-technology products

Development of

- High density and fast
- Low cost
- Non-volatile
- Lower power consumption

Memory devices



Conventional memory techonologies

Volatile RAMs

- SRAM
- DRAM

Largest part of the semiconductor memory market

ROMs

- WROM
- UVEPROM
- EEPROM
- FLASH

Some important disadvantages

DRAM
- Volatility
- Power consumption

SRAM
- Volatility
- High cost/bit

FLASH
- Limited program time (ms)
- High cost/bit
- Large programming voltages (> 10 V)

Emerging memory techonologies

The focus of research is on obtaining *non-volatile*, *fast*, *high-density*, *low-power consumption*, *high data transfer rate* and *reliable* **memory devices**.

- **FRAM**
- **MRAM**
- **PRAM**
- **RRAM**

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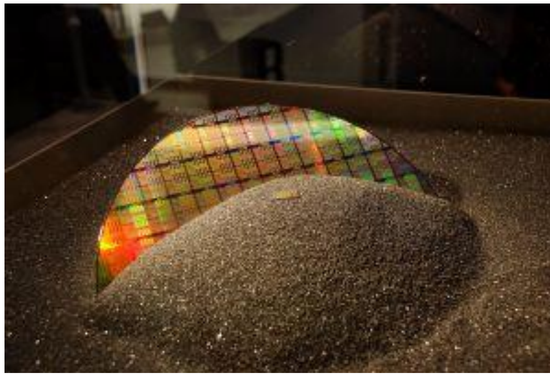
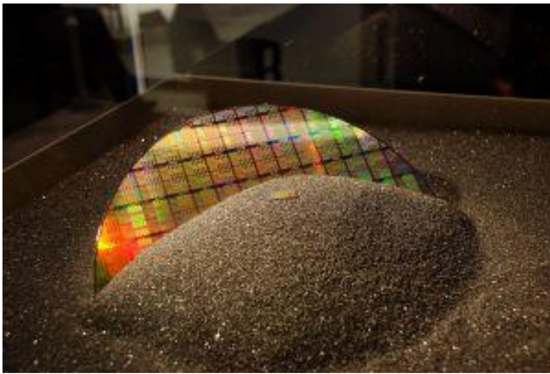
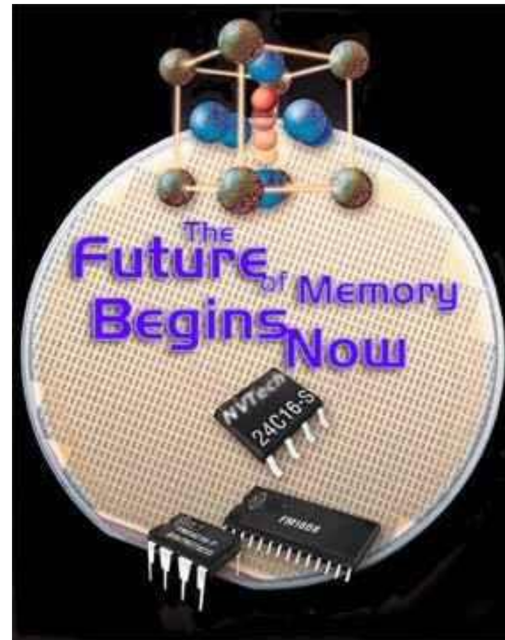


Inorganic electronics

Emerging memory techonologies

The focus of research is on obtaining *non-volatile, fast, high-density, low-power consumption, high data transfer rate* and *reliable* **memory devices**.





Inorganic electronics Towards **Organic electronics**

Emerging memory techonologies

The focus of research is on obtaining *non-volatile, fast, high-density, low-power consumption, high data transfer rate* and *reliable* **memory devices**.

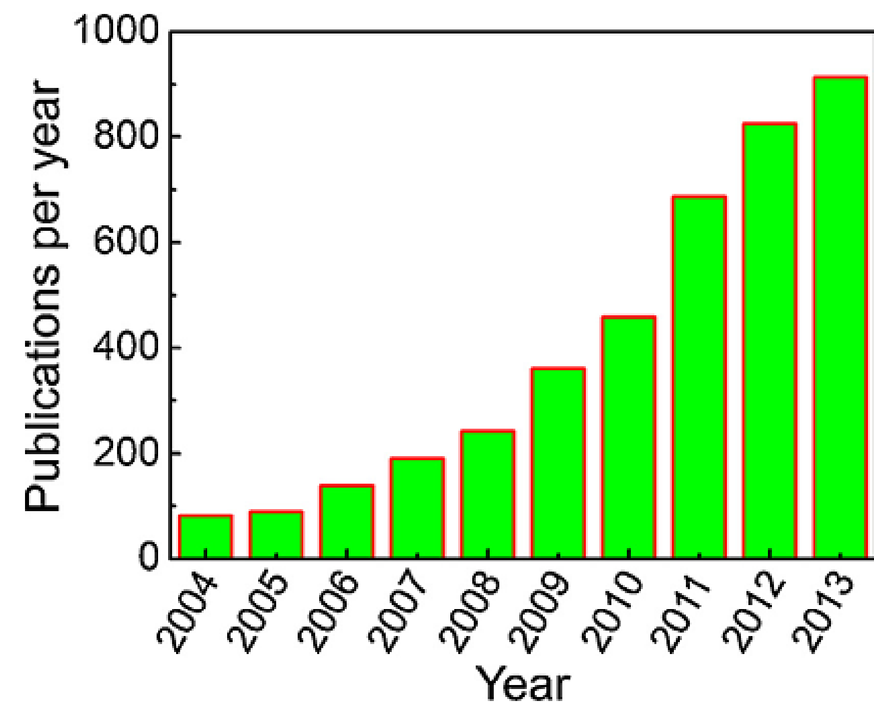
Why Organic Electronics?

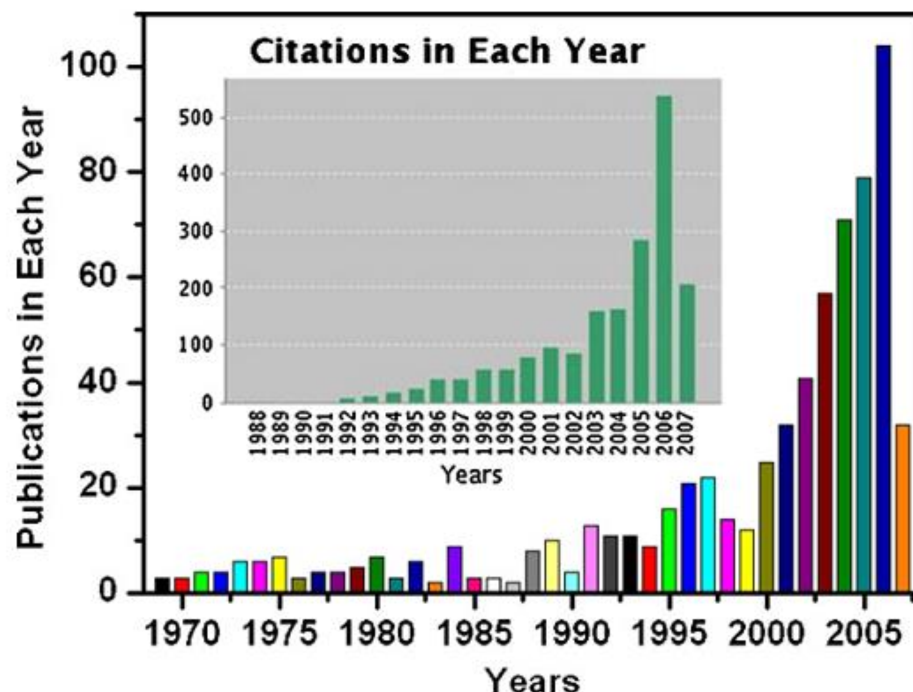
- simple fabrication
- low cost manufacturability
- mechanical flexibility and stretchability
- low-temperature fabrication process
- printability for mass industrial production

Organic electronics

Potential and challenges of organic memory devices

- ✓ Polymer electronic memories were first reported in 1970: from then, a wide variety of polymers have been reported to show memory behavior
- ✓ Many of the earlier memory effects showed unsatisfactory performance for practical application
- ✓ A rapid growth in the interest in organic memories in the last 15 years

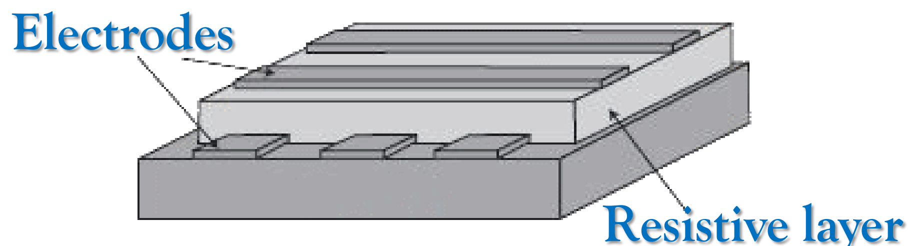




Organic memory structures

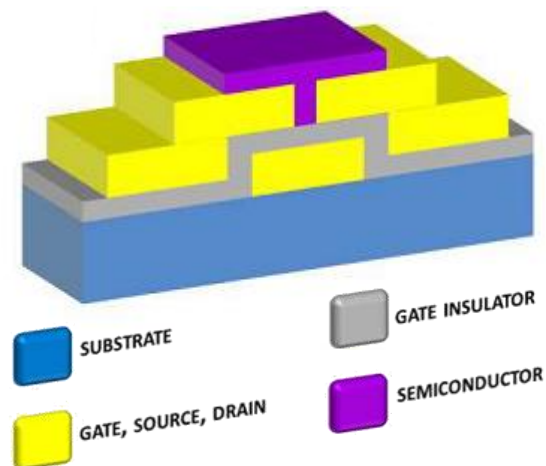
Organic memory devices that have so far appeared in the literature:

- **two-terminal bi-stable devices (resistive memories)**



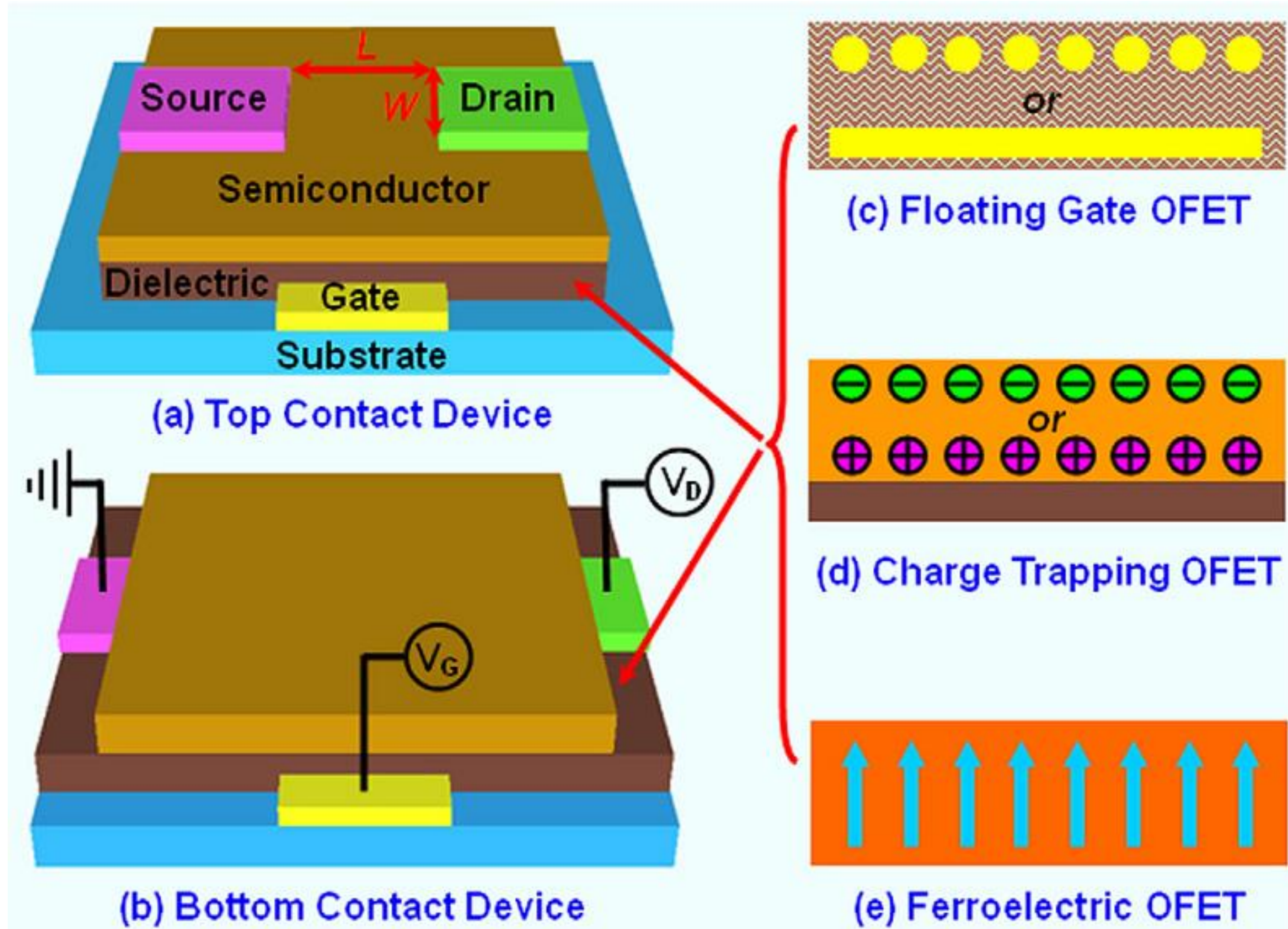
Resistance can be (reversibly) switched between low and high states (***resistive switching***) by appropriate voltage pulses

- **three-terminal devices (transistor memories)**



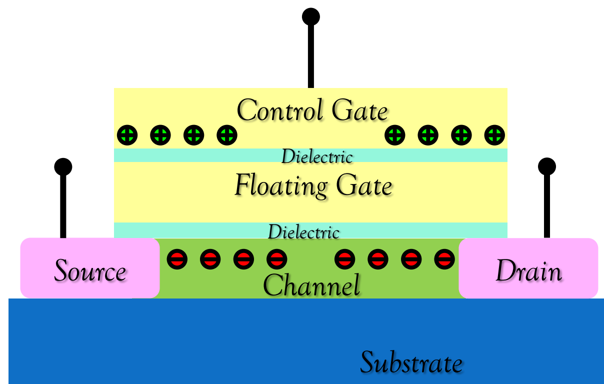
Memory effect is obtained by inducing charge storage in different areas of the device, thus resulting in a shift of the threshold voltage or hysteresis in the transfer curve.

Organic Transistor-type memories

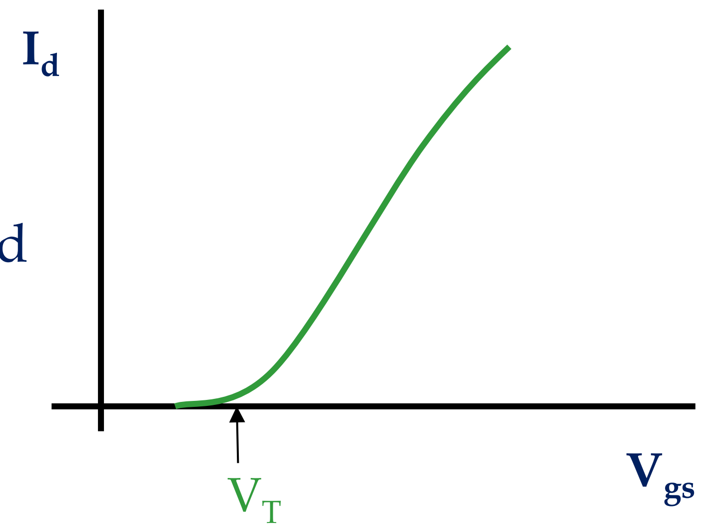


Floating gate OFET memories

Working principle



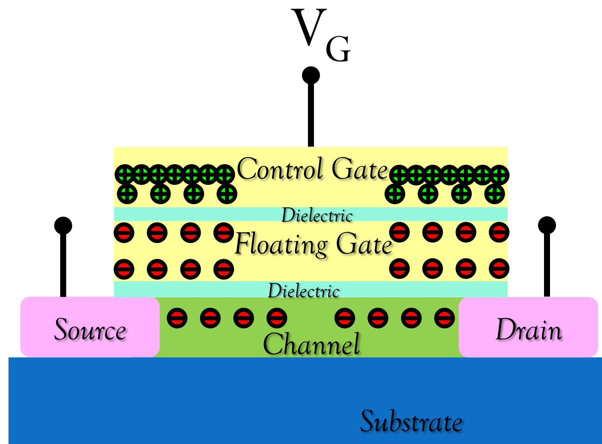
Unprogrammed



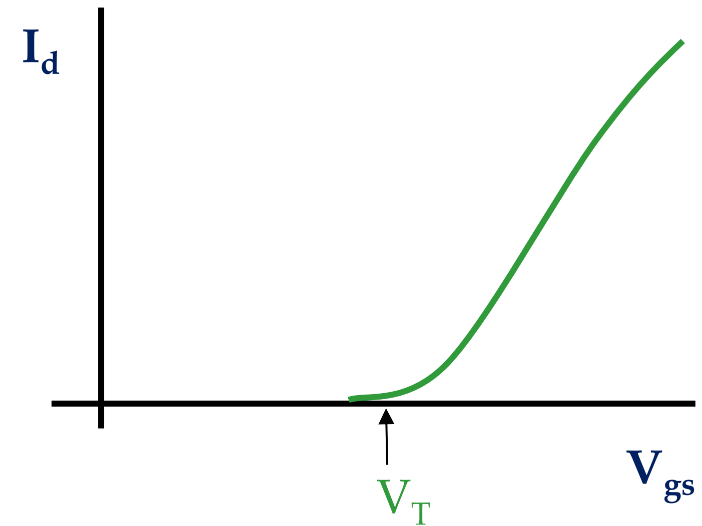
- The **dielectric layer between the floating gate and the semiconductor** must be **very thin** in order to allow injection of charges toward the floating gate
- The **dielectric layer between the floating gate and the gate** electrode must be **thick enough** to prevent discharge when V_G is removed.

Floating gate OFET memories

Working principle



Programmed



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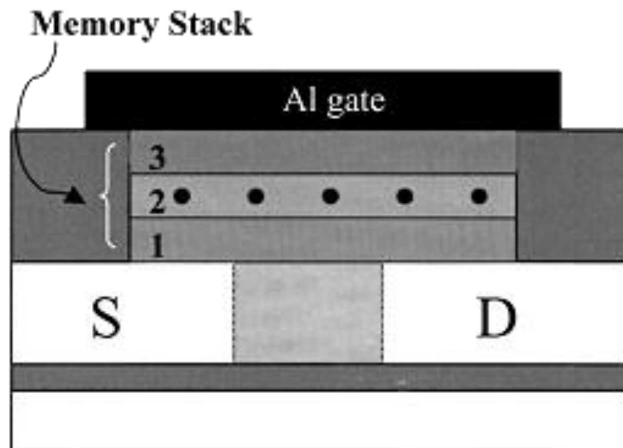
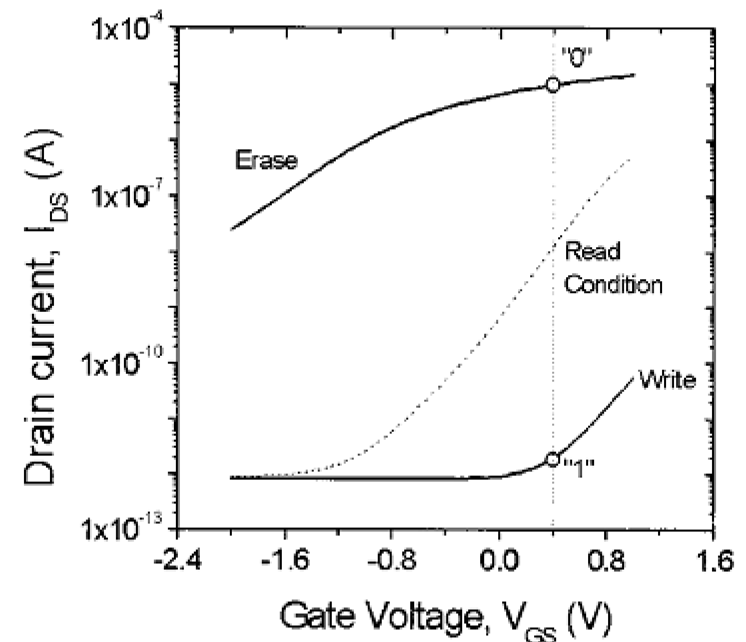
Floating gate OFET memories

2003

- Hybrid silicon–organic memory device using gold nanoparticles as charge storage elements
- Nanoparticles are separated from the silicon channel by a SiO_2 layer and from the gate electrode by an **organic insulator**



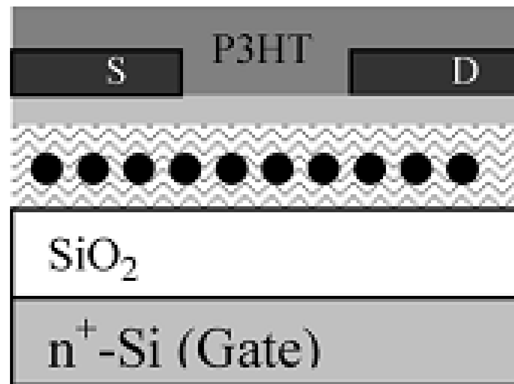


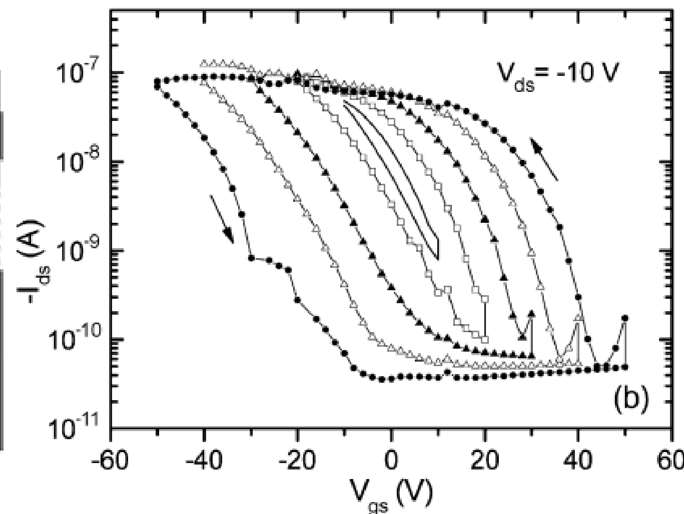
Kolliopoulou et al., Journal of Applied Physics, 94(8):5234–5239, 2003.

Floating gate OFET memories

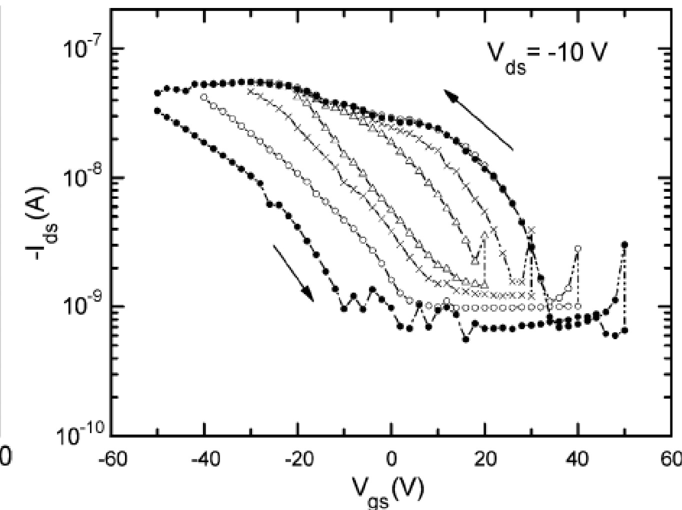
2006

- Integration of a gold nanoparticles film into the gate dielectric of an OFET to produce memory effects
- Gold nanoparticles behave as the floating gate for charge storage
- Charge storage in the Au NPs is confirmed by comparing the electrical characteristics with those of the Au NP-free
- Retention time: 200 seconds





Device with Au NPs



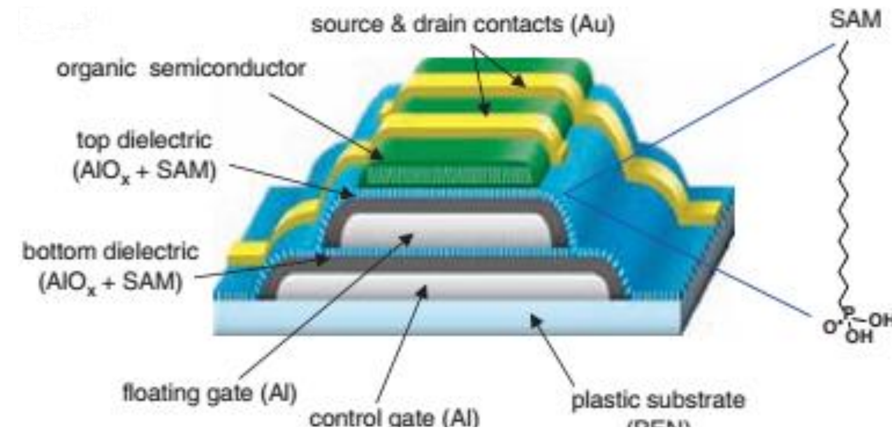
Device without Au NPs

Liu et al., Nanotechnology, IEEE Transactions on, 5(4):379–384, July 2006

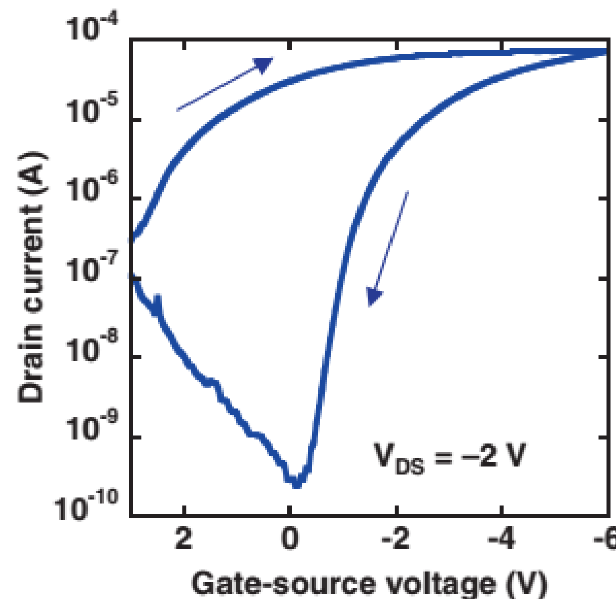
Floating gate OFET memories

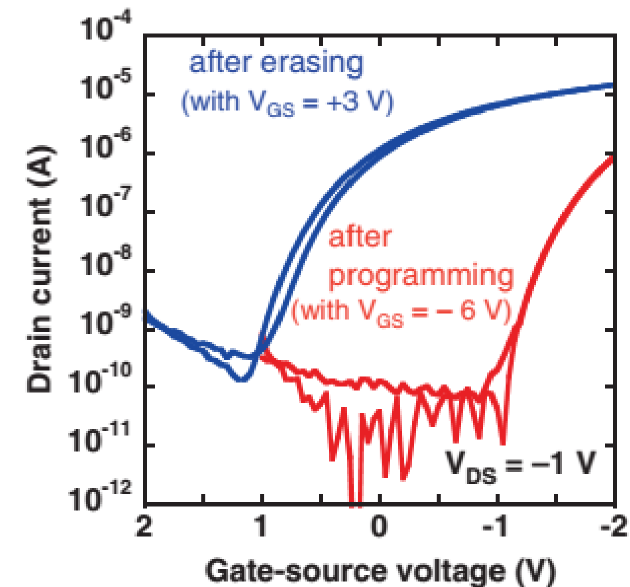
2009

- Flexible floating gate transistors with small programming voltages (-6 V to +3 V)
- Control and floating gate made of aluminum



- Dielectric made of an aluminum oxide layer and a SAM
- One of the **best result** reported to date for floating gate OFET memories
- Retention time: 12 hours

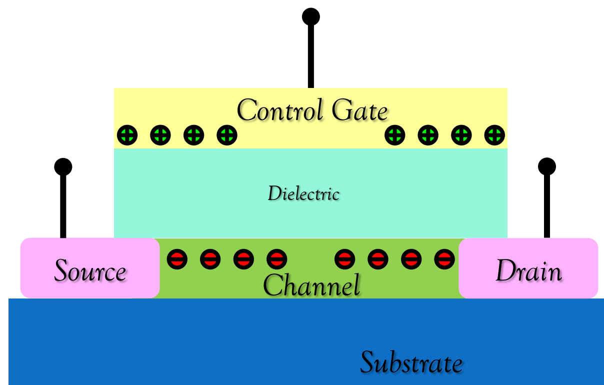




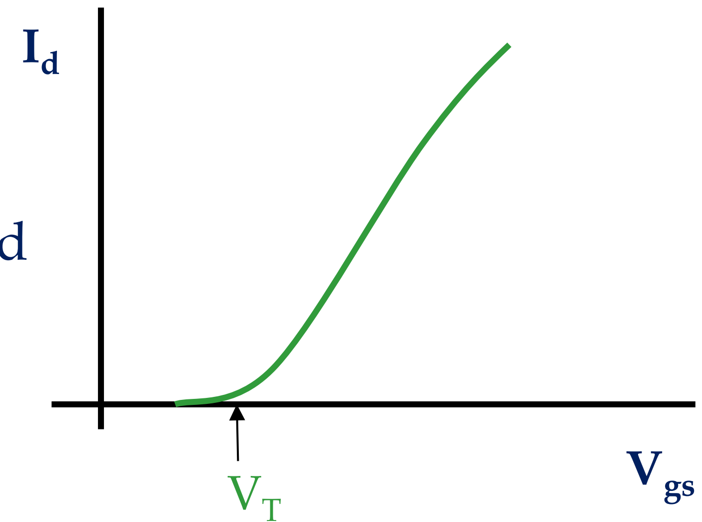
Sekitani et al., Science, 326(5959):1516–1519, 2009

Charge-trapping OFET memories

Working principle



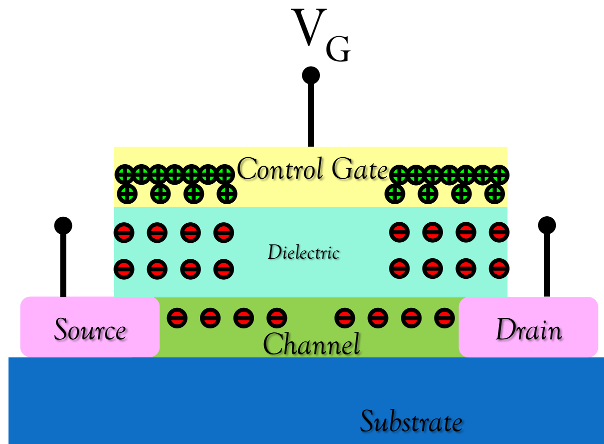
Unprogrammed



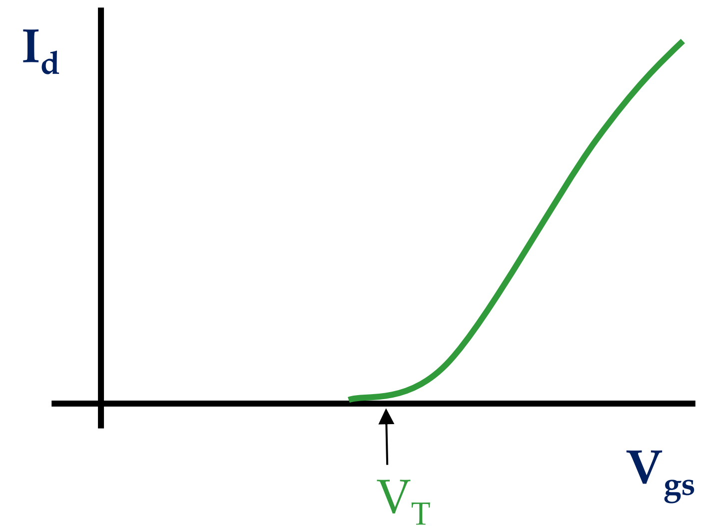
- **Charge carrier** is **stored** in an appropriate **dielectric layer (electret)** which has a quasi – permanent electric charge or dipolar polarization

Charge-trapping OFET memories

Working principle



Programmed

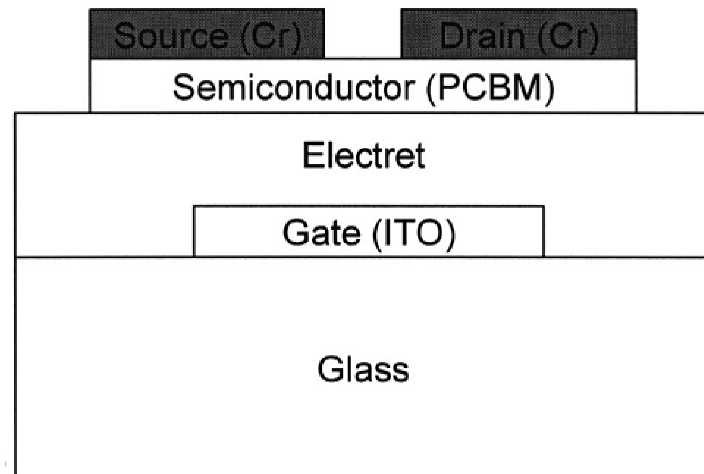


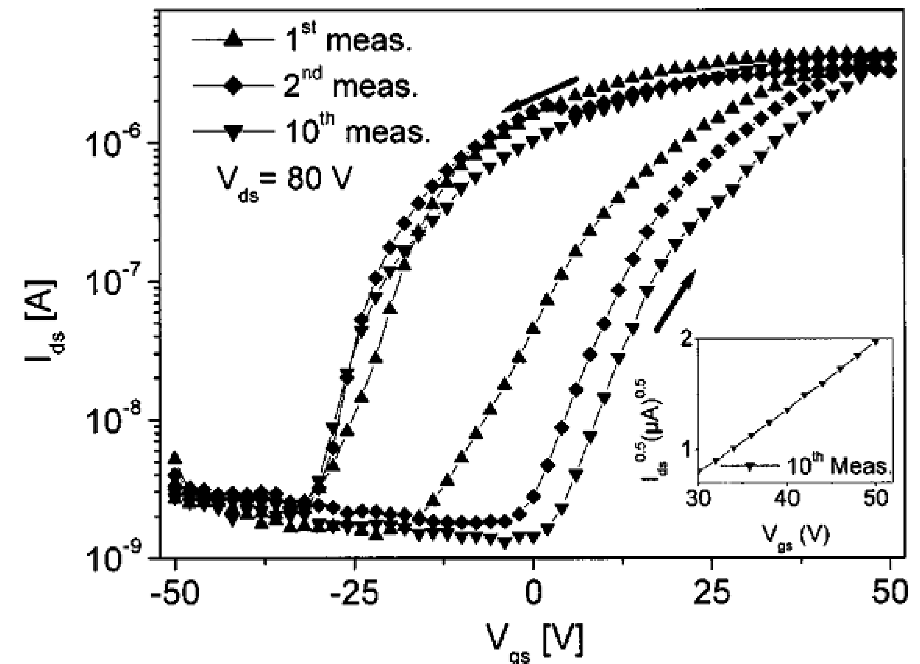
- **Charge carrier** is **stored** in an appropriate **dielectric layer (electret)** which has a quasi – permanent electric charge or dipolar polarization

Charge trapping OFET memories

2004

- First OFET memory containing an electret as gate insulator (Polyvinyl alcohol or PVA)
- Large hysteresis in the transfer characteristics cycling the gate voltage
- Retention time: 15 hours



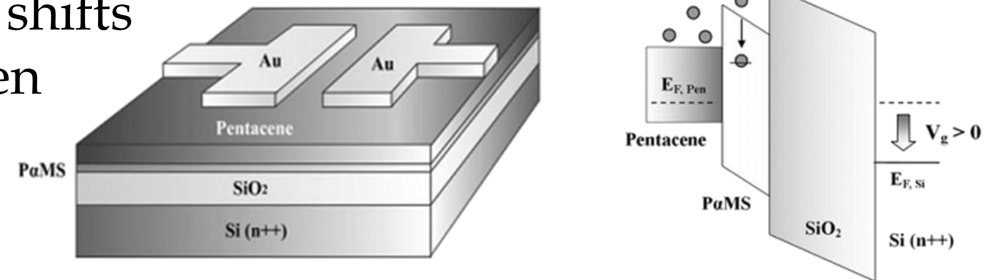


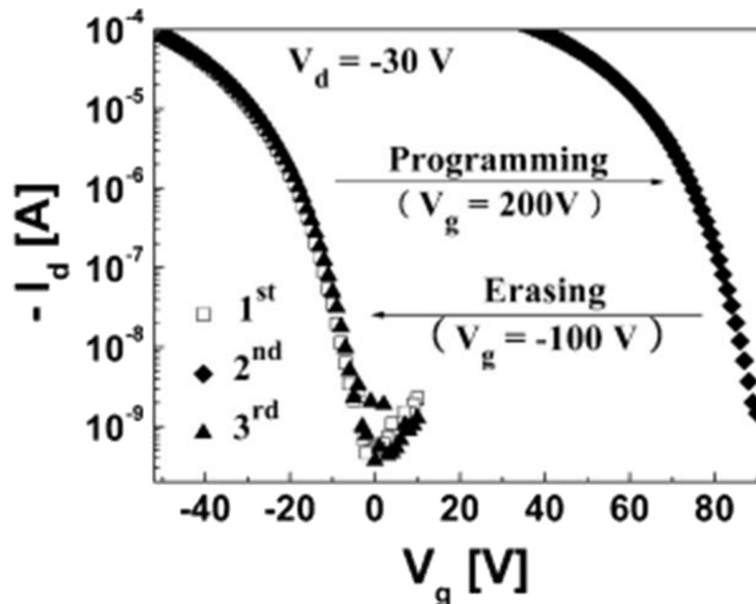
Singh et al., Applied physics letters, 85(22):5409–5411, 2004.

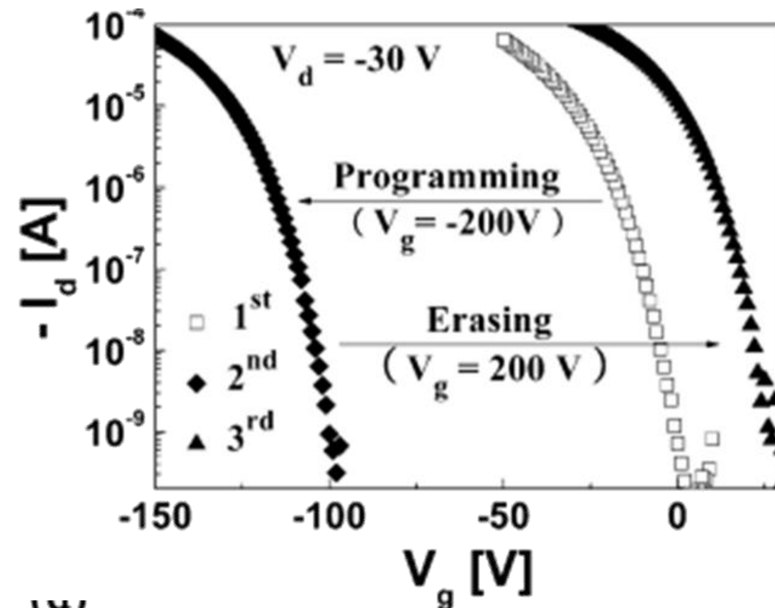
Charge trapping OFET memories

2006

- **By-layer dielectric**: hydrophobic polymer PαMS and SiO_2
- Positive and negative direction shifts
- Shifts can be obtained only when PαMS is inserted between SiO_2 gate insulator and the channel
- Retention time: 100 hours





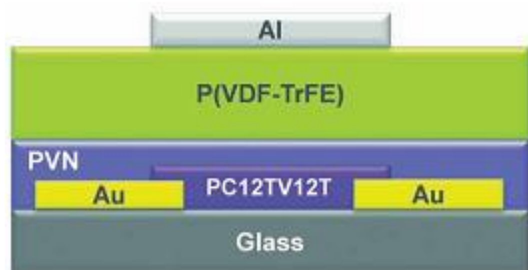


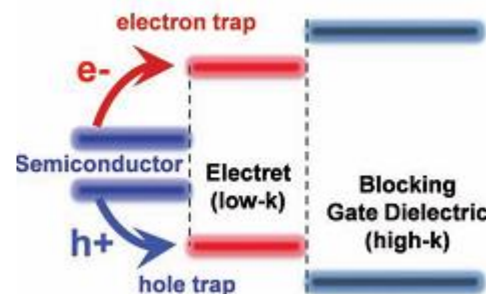
Baeg et al., Advanced Materials, 18(23):3179–3183, 2006.

Charge trapping OFET memories

2012

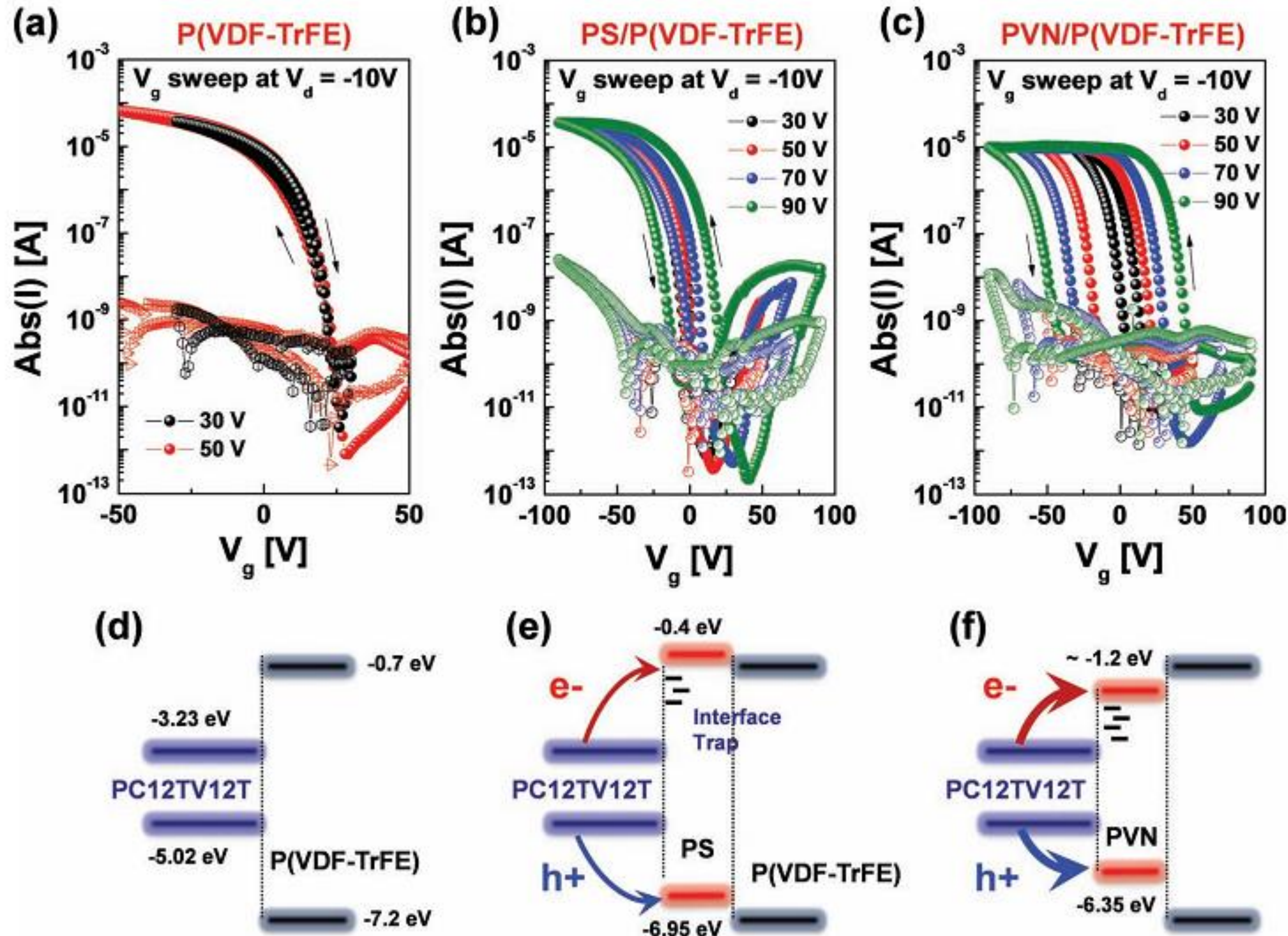
- High-performance top-gated OFET memory with **bylayered polymer dielectrics** (P(VDF-TrFE) and PVN or PS)
- Excellent non-volatile memory characteristics with P(VDF-TrFE)/PVN dielectric: high ON/OFF current ratio(∽ 10^5), a relatively low operation voltage of less than 20 V, and a long retention time of ∽ 10^7 s (less then 4 months)
- Efficient and reversible charge trapping and release in the PVN layer
- Memory characteristics effectively disappeared replacing PVN with PS
- Different memory characteristics between devices were attributed to a **different alignment of the energy levels** for the charge transfer from the semiconductor to the PVN or PS layer





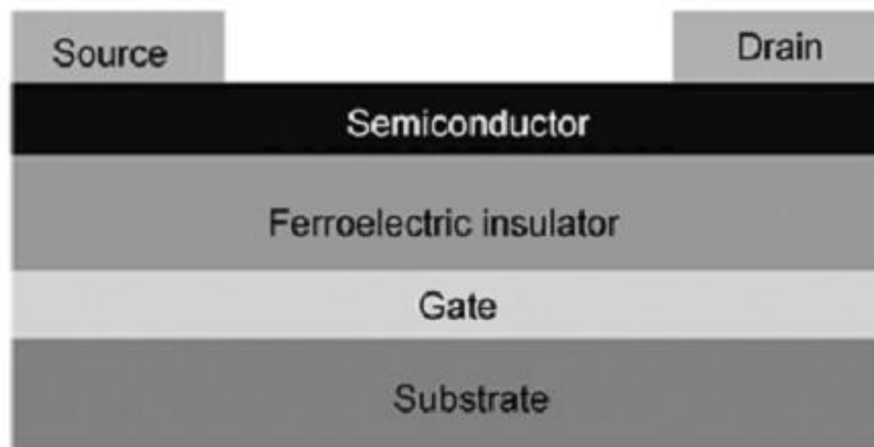
Baeg et al., Advanced Functional Materials, 22(14):2915–2926, 2012.

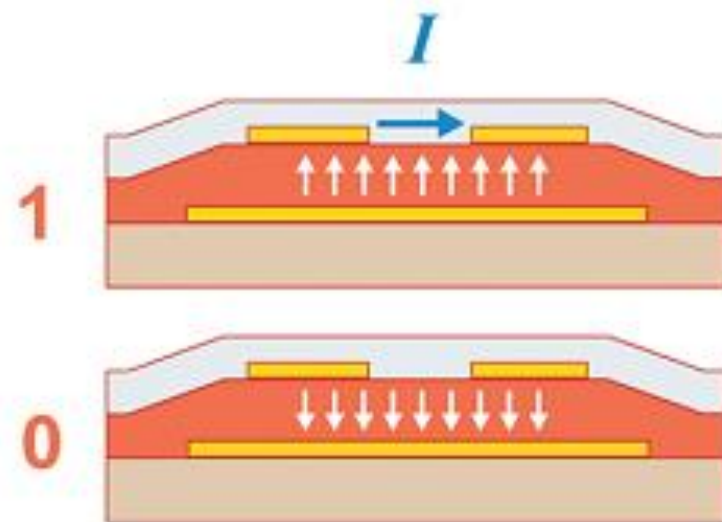
Charge trapping OFET memories



Ferroelectric OFET memories

- Ferroelectric material as gate dielectric
- Two stable polarization states: switching from one polarization state to the other can occur by applying a sufficiently large gate bias
- Depending on the direction of the polarization, positive or negative counter charges are induced at the semiconductor-ferroelectric interface, causing a positive or negative onset voltage shift of the transistor





Ferroelectric OFET memories

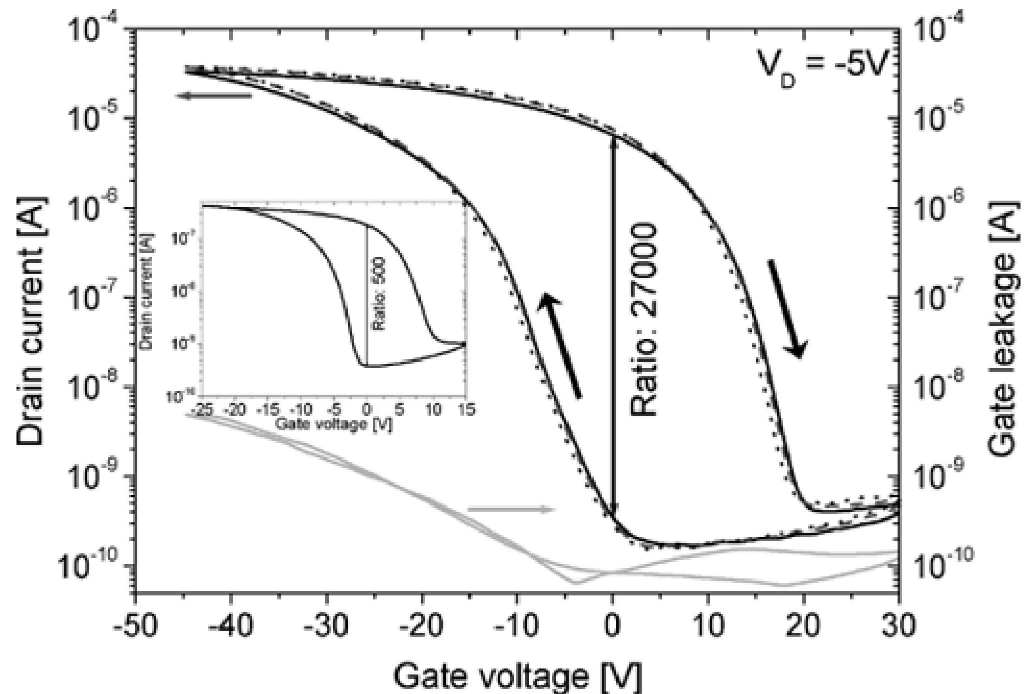
1986

- First FET based on a polymeric ferroelectric

2004-2005

- All organic FET devices incorporating a ferroelectric-like polymer as the gate insulator and pentacene as the organic semiconductor were first reported
- A clear hysteresis in transfer characteristic
- Retention time: few days

Schroeder et al., Electron Device Letters, IEEE, 26(2):69–71, Feb 2005.

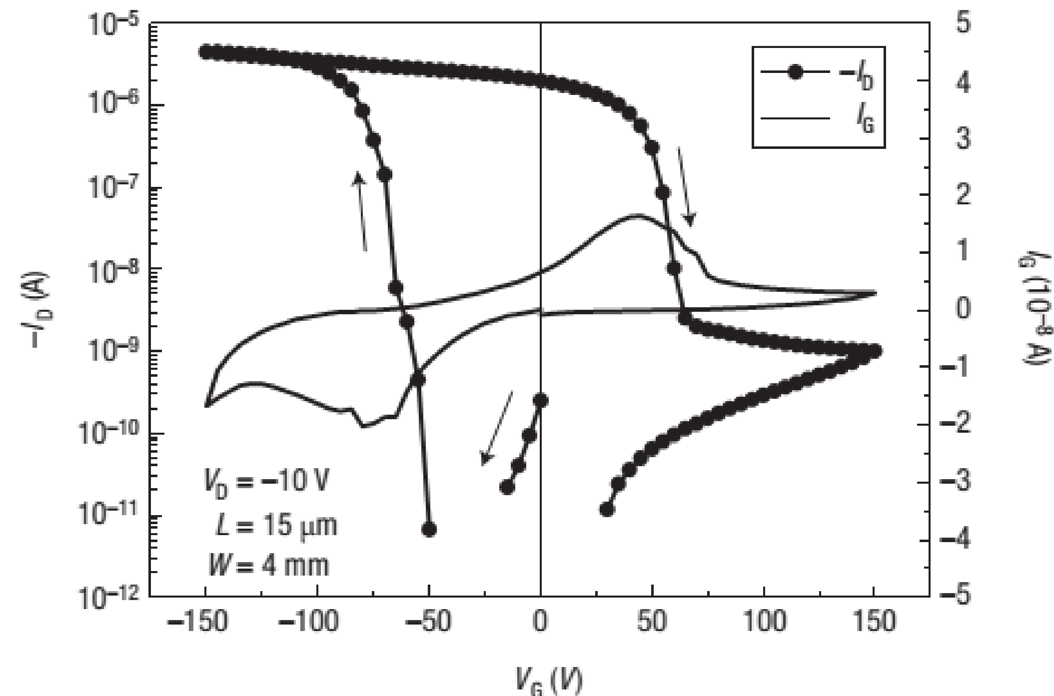


Ferroelectric OFET memories

2005

- High-performance solution-processed polymer FeFET memories consisting of P(VDF–TrFE) as the gate insulator
- Operation voltages: ± 60 V and ± 35 V (ferroelectric layer thickness of 1.7 and 0.85 μm)
- Retention time: 1 week

The application of a negative gate bias results in a sharp increase by several orders of magnitude of the channel current associated with hole accumulation and a remanent on-state current after bringing the bias back to zero.



Naber et al., Nature Materials, 4(3):243–248, 2005.

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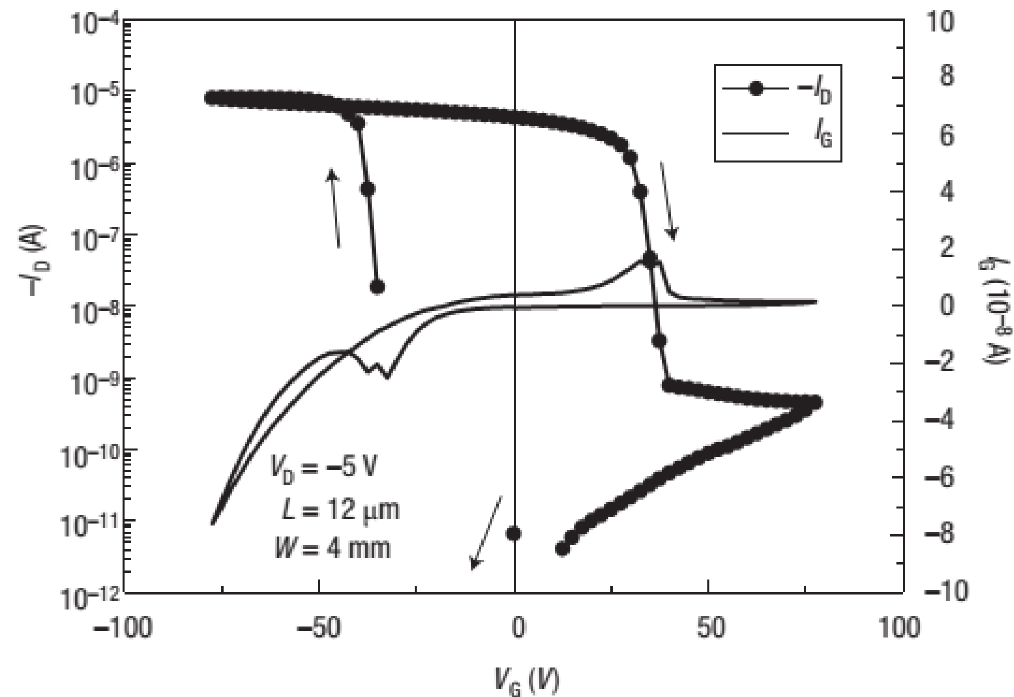
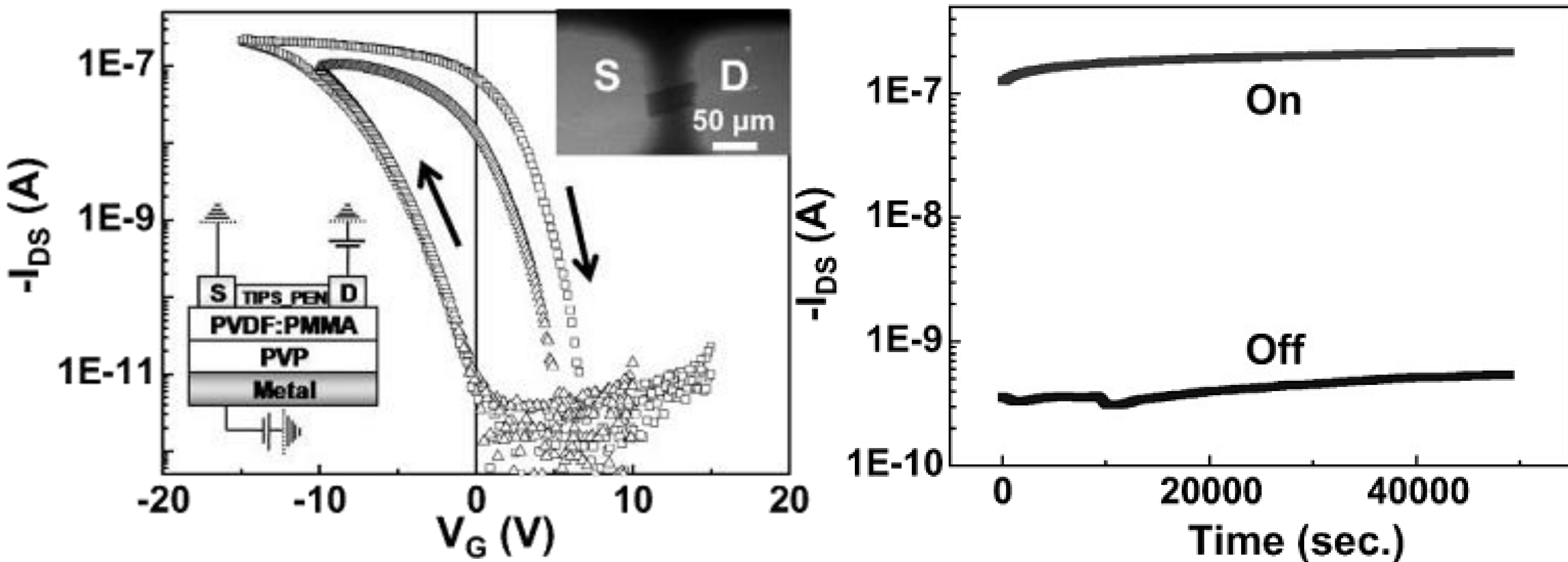


Naber et al., Nature Materials, 4(3):243–248, 2005.

Ferroelectric OFET memories

2009

- Bottom gate FeFET containing PVDF/PMMA blend films of 200 nm
- Operation voltages: 15 V
- Retention time: 15 h



Kang et al., Advanced Functional Materials, 19(17):2812–2818, 2009.

Developmental status

- Tremendous progress has been made in the field of OFET memories since it was first described.
- OFET memories have great potential for application in low cost, large areas, plastic systems, but many challenges are still open:
  - program/read/erase voltages are still large;
  - data retention times are too short to satisfy the requirements of practical applications;
  - operating mechanisms of OFET memories are not clearly understood.
- All of these issues need to be addressed in the future to aid the design of high performance devices.