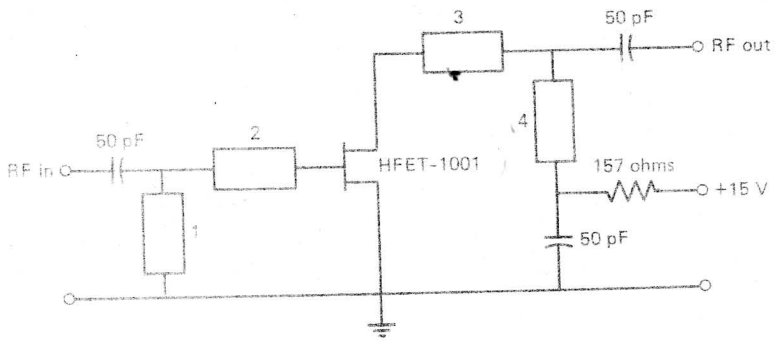

Figure 3.3 Complete amplifier schematic.

required to be flat. In the next section methods for realizing a flat VSWR will be discussed.

Notice that it is inherently impossible simultaneously to achieve flat gain, low input reflection, and low output reflection with lossless matching circuits.

The amplifier stability is checked in Fig. 3.2 for the final design over 1 to 10 GHz. Notice that the short circuited stubs have guaranteed that the Γ_G and Γ_L are on the "safe side" of the Smith Chart at low frequencies. The dc bias circuit is found from estimating $I_{DSS} \simeq 70$ mA. The schematic for the entire amplifier is given in Fig. 3.3. All elements are realizable.

3.2 Balanced Amplifiers

There are at least three techniques for improving the input and output VSWR of the amplifier while simultaneously presenting the correct Γ_G and Γ_L to the transistor terminals. The most popular technique is that shown in Fig. 3.4*a*, the use of 3-dB Lange couplers in a balanced configuration. In this technique the reflections from the identical amplifiers all appear at the termination port, so that the input port appears matched.

One can show that

$$S_{11} = \tfrac{1}{2}(S_{11A} - S_{11B}) \tag{3.1}$$

The operating bandwidth of the amplifier is limited by the bandwidth of the coupler, which can be made very wide (more than 2 octaves). This technique of building one-stage balanced amplifiers has many advantages:

1 The transistor can be intentionally mismatched for gain flatness, noise figure, output power, stability, and so on.

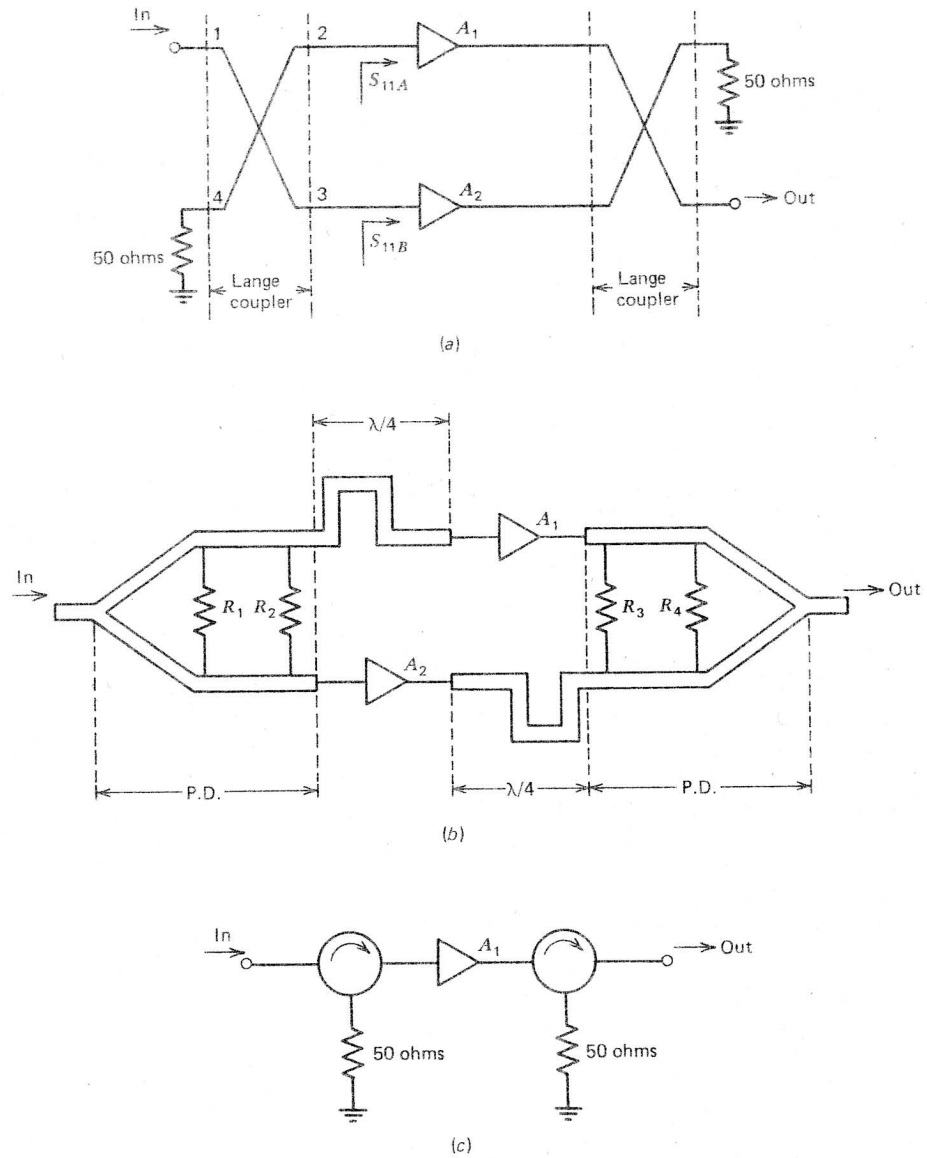

Figure 3.4 Low-VSWR amplifiers, (*a*) Balanced amplifier using 3-dB Lange coupler; (*b*) Balanced amplifier using 3-dB Wilkinson power divider (P.D.); (*c*) Isolator amplifier.

2 Each stage is isolated from the following stage by the Lange couplers. Very little interstage tuning is needed.
3 The reflections from A_1 and A_2 are terminated in 50 ohms, which usually guarantees stability.
4 If one transistor fails, the operating gain drops about 6 dB, which can be a useful feature in some applications.
5 The linear output power is 3 dB higher.
6 The labor in tuning these amplifiers is much less than in designing and tuning multistage unbalanced amplifiers.

The disadvantages of balanced amplifiers are the higher cost of more transistors and the higher dc power requirement.

Another popular choice for balanced amplifiers is the 3-dB Wilkinson power divider circuit shown in Fig. 3.4*b*. The power is split in phase, and a quarter-wave line is inserted in front of one amplifier and behind the opposite amplifier. If the input reflection coefficients S'_{11} of the amplifiers are identical, all reflected input signals appear 180° out of phase across R_2 and are dissipated. A low-frequency termination is also provided by R_2 for the sake of stability. Similarly, the output is terminated in R_3, and the signals are added in phase at the output. This technique will require more space than the Lange coupler and gives less bandwidth. The advantage is that a much simpler microstripline circuit can be used (no narrow coupling strips).

The relative bandwidths of these two approaches are shown in Fig. 3.5. At present the single-section Lange coupler is the most popular choice for double-octave wideband amplifiers. For wide bandwidths, the coupling is

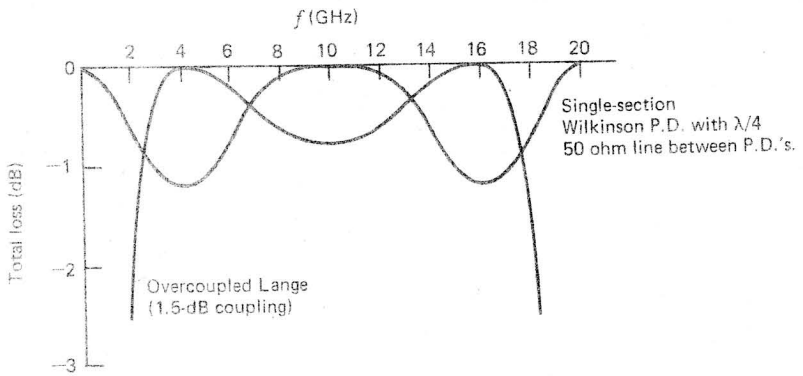

Figure 3.5 Comparison of 10-GHz cascaded Lange couplers versus cascaded single-section Wilkinson power dividers.

tighter than 3 dB (about 1.5 dB seems optimum). The third approach to low-VSWR amplifiers is the use of broadband isolators. This approach requires a thin-film ferrite circuit and a magnetic structure for realizing the isolators. Moreover, low-frequency broadband isolators are not available below 2 GHz. Unless a proven isolator capability exists, this approach is not commonly used.

In summary, the most common amplifier designs use the 3-dB Lange coupler to achieve low VSWR over broad bandwidths. These balanced amplifiers are easily cascaded to achieve high gain and high output powers.

3.3 Low-Noise Design

For the low-noise design the transistor data must include the S-parameters at the low-noise bias and four noise parameters. One common noise parameter set is

$F_{\min}$	Minimum noise figure
$R_n = N/G_G$	Noise resistance
$Y_{on} = G_{on} + jB_{on}$	Optimum noise admittance

The noise figure of the two-port is given by the source admittance (or impedance) presented to the input terminals and is calculated from (1.182), which is repeated here:

$$F = F_{\min} + \frac{R_n}{G_G}|Y_G - Y_{on}|^2$$

The output port is tuned for the maximum available gain if the amplifier is single-stage. In a two-stage, low-noise design the interstage circuit will probably be tuned for minimum second-stage noise figure. The noise figure of a multistage amplifier is given by

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_{av1}} + \frac{F_3 - 1}{G_{av1}G_{av2}} + \cdots \tag{3.2}$$

where G_{av1} = available gain of first stage
G_{av2} = available gain of second stage

If all stages are designed for minimum noise figure, we find

$$(F_{tot})_{\min} = (F_{\min} - 1) + \frac{F_{\min} - 1}{G_{av}} + \frac{F_{\min} - 1}{(G_{av})^2} + \cdots + 1 \tag{3.3}$$