thin (some large chips are thinned to from 0.001 to 0.002 inches), and often a thick gold layer must be plated onto the chip's underside. The resulting thermal resistance between the channel and the mounting surface may be from 1 to 2 W/°C (in the case of a large chip) to 50 W/°C or more (for single-cell, medium-power devices). The resulting increase in channel temperature may be several tens of degrees C at full power.

9.1.2 Modeling Power MESFETs

Because the FET power amplifier is a large-signal component, we use the large-signal model of the MESFET described in Section 2.4.2. The lumped quasistatic equivalent circuit is shown in Figure 2.16; this circuit includes three nonlinear elements (C_g, C_d, and I_d), all of which are functions of the gate and drain voltages, V_g and V_d, respectively. It is important to note that MESFETs are often driven into their linear regions (to drain voltages below the knee of the I/V curve) when used in power amplifiers; therefore, when we calculate amplifier performance, it is often important to include the voltage dependence of C_d, which varies most strongly when the device enters its linear region. The resistances and the drain-source capacitance, C_{ds}, are treated as linear elements. Gate and drain inductances and package parasitics, not shown in Figure 2.16, can sometimes be included in the source and load networks. If not, they must be included in the complete model.

It is a common practice to use the empirical form of $I_d(V_g, V_d)$ of (2.4.5) in power-amplifier analyses. It is often helpful to modify (2.4.5) to include the dependence of V_t, the MESFET's turn-on voltage, on V_d via an appropriate empirical expression. $C_g(V_g, V_d)$ is often modeled as an ideal Schottky-barrier capacitance (i.e., independent of V_d), although it is sometimes worthwhile to modify the ideal characteristic of (2.3.5) to account for the drop in capacitance when $V_g < V_t$. Modeling the dependence of C_d on V_g and V_d is somewhat more difficult; usually an empirical expression must be used. Reference 9.1 is a good example of an intelligent approach to the modeling of power MESFETs.

Although Figure 2.16 describes a single-cell device, the same circuit can be used to describe a multicell device. If the multicell device has N identical cells and there are no additional parasitics, we need only divide the resistances of a single cell by N and multiply the capacitances and I_d by N to generate the multicell model. It is usually valid to assume that the cells of a multicell device are identical. However, in practice, we can rarely ignore the parasitic capacitances and inductances associated with

air bridges or other overlay metalizations and not part of the individu cells. Often, some of these parasitics can be absorbed into the source ai load impedances or into other circuit elements. Nonetheless, because the large capacitances and small resistances of multicell power device directly measuring the S parameters of large devices is difficult; cons quently, large devices are usually modeled by scaling measurements their individual cells.

Because power MESFETs are often operated at elevated chann temperatures, their I/V and C/V characteristics and S parameters me sured at room temperature may not be valid. Therefore, it is worthwhi to attempt to measure the nonlinearities as close to the operating ten perature as possible.

9.2 FUNDAMENTAL CONSIDERATIONS IN POWER-AMPLIFIER DESIGN

Figure 9.1 shows a simplified circuit of a FET power amplifier. W will derive some of the fundamental properties and limitations of powe amplifiers via this circuit. The circuit consists of a MESFET, excitatio and gate-bias sources, a tuned circuit, and load, R_L. The drain-bias voltag is V_{dd}, and the gate bias is adjusted so that, in the absence of excitatio the dc drain current is I_{dd}. Initially, we will assume that the MESFET an ideal transconductance amplifier, that it has no resistive or reactiv parasitics (so $V_{gs} = V_g$ and $V_{ds} = V_d$) and that the tuned circuit is resonar at the excitation frequency.

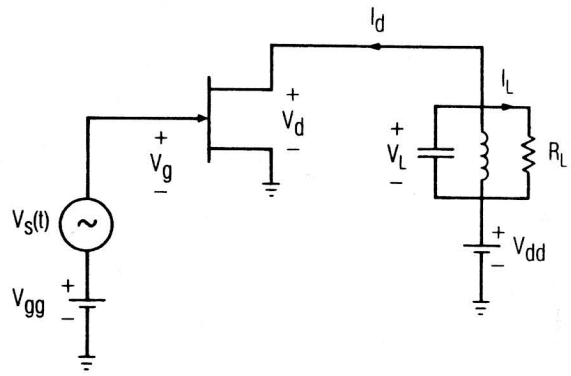

Figure 9.1 Equivalent circuit of an ideal FET power amplifier.

The application of a sinusoidal excitation $V_s(t)$ to the gate generates an RF component of drain current, $\Delta I_d(t)$. If the tuned circuit is resonant at the RF frequency, that current must pass entirely through R_L. The RF component of the drain voltage, $\Delta V_d(t)$, is equal to the voltage drop across R_L; that is:

$$V_L(t) = \Delta V_d(t) = -\Delta I_d(t) R_L \tag{9.2.1}$$

Each curve in the MESFET's drain I/V characteristic, shown in Figure 9.2, represents a range of values of V_d and I_d that can exist when the gate voltage, V_g, has a specified value; (9.2.1) expresses an additional constraint on V_d and I_d. Thus, the drain voltage and current must simultaneously satisfy both (9.2.1) and the I/V curve for V_g; these values of V_d and I_d are found at the point where the I/V curve and (9.2.1) intersect. Figure 9.2 shows (9.2.1) plotted on top of the MESFET's drain I/V curves; when the FET is excited by $V_s(t)$, $V_d(t)$ and $I_d(t)$ must always lie along the straight line, called a *load line*.

In a power amplifier, we wish to maximize the power delivered to R_L. This power is clearly maximum when both $V_L(t) = \Delta V_d(t)$ and $I_L(t) = -\Delta I_d(t)$ have their maximum excursions. If we recognize that V_d and I_d can not be less than zero, these maximum excursions occur when $|V_L(t)| = V_{dd}$ and $|I_L(t)| = I_{dd}$; the geometry of the load line dictates that these conditions are met when $R_L = V_{max,A}/I_{max} = V_{dd}/I_{dd}$. Then, if $V_s(t)$ and V_{gg} are chosen appropriately, the drain voltage varies from zero to $V_{max,A} = 2V_{dd}$, and the drain current varies from zero to $I_{max} = 2I_{dd}$. The $V_d(t)$ and $I_d(t)$ waveforms in this case are shown in Figure 9.3.

The output power, P_L, under these conditions is

$$P_L = 0.5\,|V_L(t)|\,|I_L(t)| = 0.5\,V_{dd}\,I_{dd} \tag{9.2.2}$$

Usually, we wish to maximize the output power of a specified transistor. In this case, $V_{max,A}$ and I_{max} are the devices's maximum drain voltage and current, and the maximum output power is

$$P_L = \frac{1}{2}\left(\frac{1}{2}V_{max,A}\right)\left(\frac{1}{2}I_{max}\right)$$

$$= \frac{1}{8}V_{max,A}\,I_{max} \tag{9.2.3}$$

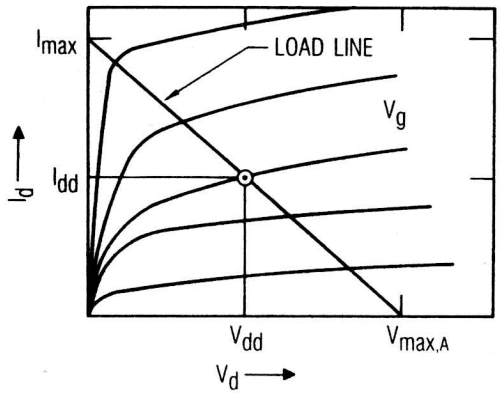

Figure 9.2 Drain I/V characteristics and the load line of the MESFET in Figure 9.1.

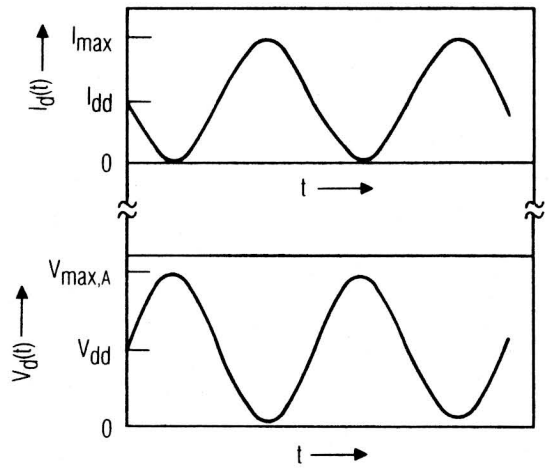

Figure 9.3 Drain voltage and current waveforms in the ideal Class-A FET power amplifier; the bias voltages, excitation, and load resistance are chosen optimally, causing both $I_d(t)$ and $V_d(t)$ to vary between zero and their maximum values.

The dc current remains constant at I_{dd} at all excitation levels; therefore, the dc power $P_{dc} = V_{dd}I_{dd}$ an the dc-RF conversion efficiency is

$$\eta_{dc} = \frac{P_L}{P_{dc}} = \frac{0.5V_{dd}I_{dd}}{V_{dd}I_{dd}} = 50 \text{ percent} \tag{9.2.4}$$

An amplifier operated in this manner is called a *Class-A amplifier* (although this arcane terminology was originally used to describe vacuum-tube amplifiers, it has been transferred with little modification from vacuum tubes to bipolar transistors and finally to MESFETs). In theory the maximum efficiency of such an amplifier is 50 percent, so the transistor in a Class-A amplifier dissipates at least as much power in the form of heat as it delivers to the RF load.

Two factors complicate this simple reasoning. The first is that it is not possible in practice to vary the drain voltage and current all the way to the peak of the load line, where $I_d = I_{max}$ and $V_d = 0$, because of the knee in the uppermost *I/V* curve in Figure 9.2. The result of this limitation is that $|V_L(t)|$ cannot quite equal V_{dd}, and $|I_L(t)|$ must be less than I_{dd}, so both the output power and efficiency are somewhat lower than the values given by (9.2.3) and (9.2.4). The second is that the MESFET is nonlinear, so the $I_d(t)$ waveform is generally not sinusoidal. The tuned circuit constrains $I_L(t)$ to be sinusoidal, however, so the assumption that $I_L(t) = -\Delta I_d(t)$ is not precisely correct and in fact $|I_L(t)| < |\Delta I_d(t)|$, which further limits output power and efficiency. Nevertheless, because the purpose of this derivation is to illustrate fundamental properties of power amplifiers, we will continue to assume that $I_d(t)$ can reach I_{max} and that the FET is linear. We will modify these assumptions when we face the problem of accurately designing practical power amplifiers.

Two undesirable characteristics of the Class-A amplifier are its relatively low efficiency and its dissipation of a great amount of power even when it is not excited; in fact, Class-A amplifiers dissipate more power under quiescent (unexcited) conditions than when they are operating. Thus, a Class-A amplifier must be disigned either to safely dissipate its quiescent power or to be turned off when not in use. Both alternatives are unacceptable in many applications.

Many of the disadvantages of Class-A operation are circumvented by Class-B operation. The gate-bias voltage of an ideal Class-B amplifier is set at the turn-on voltage V_t; therefore, the FET's quiescent drain current is zero, so the FET dissipates no power in the absence of excitation. The bias point is thus V_{dd} on the voltage axis of the FET's *I/V* curves. It is not possible to draw a true load line describing the single-device amplifier in

Figure 9.1 when the amplifier is biased to achieve Class-B operation because the harmonic components of I_d, which are substantial in a Class-B amplifier, do not circulate in R_L; therefore, (9.2.1) is not valid here.

During the half cycle, when $V_s(t)$ is positive, $V_g(t) > V(t)$ and the drain conducts; during the other half cycle, $V_g(t) < V_t$ and the drain current is zero. The drain current $I_d(t)$ is therefore a pulse train, and each pulse has the half-cosine shape shown in Figure 9.4. The dc drain current is the average value of the half-cosine waveform. From Fourier analysis, we find that, under full excitation, $I_{dc} = I_{max}/\pi$, and the amplifier's dc power is

$$P_{dc} = V_{dd}\frac{I_{max}}{\pi} \tag{9.2.5}$$

Because the tuned circuit allows only the fundamental and dc components of drain voltage to exist, the ac part of $V_d(t)$, which is equal to $V_L(t)$, is a continuous sinusoid. The tuned circuit also allows only the fundamental component of $I_d(t)$ to pass through R_L. The power delivered to the load is:

$$P_L = 0.5I_1\,|V_L(t)| \tag{9.2.6}$$

where $I_1 = |I_L(t)|$ is the magnitude of the fundamental component of $I_d(t)$. From Figure 9.4, $|V_L(t)| = |\Delta V_d(t)| = V_{dd}$, and from Fourier analysis, $I_1 = 0.5I_{max}$. Then,

$$P_L = \frac{1}{2}\left(\frac{1}{2}I_{max}\right)V_{dd} = \frac{1}{4}I_{max}V_{dd} \tag{9.2.7}$$

and the dc-RF efficiency is

$$\eta_{dc} = \frac{P_L}{P_{dc}} = \frac{\pi}{4} = 0.78 \tag{9.2.8}$$

Theoretically, the Class-B amplifier has a maximum efficiency of 78 percent, much better than the 50 percent limit of the Class-A amplifier. It has achieved this improvement by allowing the channel to conduct during only half the period of the excitation; during the time that the FET is turned off, the FET dissipates no power. However, the peak value of the Class-B amplifier's drain current is twice the value of $\Delta I_d(t)$ in the Class-A amplifier, so the fundamental-frequency component of the output current is the same in both types of amplifiers.

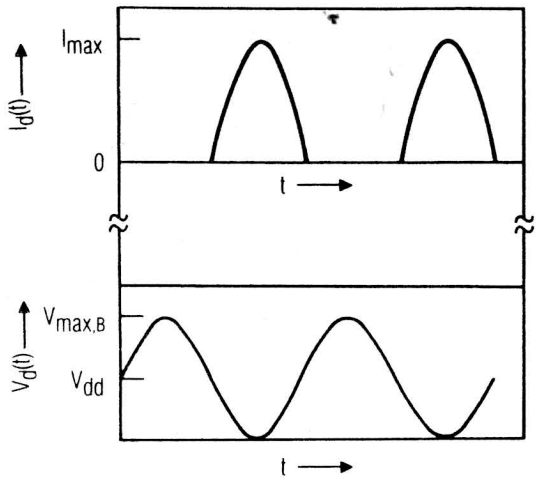

Figure 9.4 Drain voltage and current waveforms in the ideal Class-B amplifier. The drain conducts in sinusoidal pulses because the gate is biased at V_t.

To find the maximum output power in terms of the device's limitations, we let the maximum drain voltage be $V_{\max,B}$ and note that $V_{\max,B} = 2V_{dd} = 2\,|V_L(t)|$. Then,

$$P_L = \frac{1}{2}\left(\frac{1}{2}V_{\max,B}\right)\left(\frac{1}{2}I_{\max}\right) = \frac{1}{8}V_{\max,B}I_{\max} \tag{9.2.9}$$

which is the same as that of the Class-A amplifier if $V_{\max,A} = V_{\max,B}$.

In order to achieve the maximum output power, the load resistance R_L must be such that

$$I_1R_L = 0.5I_{\max}R_L = |V_L(t)| = V_{dd} \tag{9.2.10}$$

so

$$R_L = \frac{2V_{dd}}{I_{\max}} = \frac{V_{\max,B}}{I_{\max}} \tag{9.2.11}$$

and we see that the load resistance of the Class-B amplifier is the same as that of the Class-A. Furthermore, because in both amplifiers the load resistance and the fundamental component of the load current are the same, the output power must also be the same.

Because the maximum drain voltage is limited by gate-drain avalanche breakdown, $V_{\max,A}$ is always greater than $V_{\max,B}$. In the Class-A amplifier, the maximum drain-gate voltage occurs when $V_d = V_{\max,A}$ and $V_g = V_t$. Thus, if V_a is the drain-gate avalanche breakdown voltage:

$$V_{\max,A} = V_a - |V_t| \tag{9.2.12}$$

The Class-B amplifier is biased at $V_{gg} = V_t$, so the maximum negative excursion of V_g is $2V_t$. Then,

$$V_{\max,B} = V_a - 2|V_t| \tag{9.2.13}$$

so $V_{\max,B}$ is less than $V_{\max,A}$ by an amount equal to $|V_t|$. Accordingly, the maximum output power of a Class-B amplifier is slightly lower than that of a Class-A amplifier using the same device.

The difference in maximum output power between Class-A and Class-B amplifiers is not the most significant one; there is a much greater difference in their gains. The gate voltage of a Class-A amplifier varies between zero and V_t; in a Class-B amplifier the gate voltage varies between zero and $2V_t$. More input power is required to achieve the Class-B amplifier's wider gate-voltage variation but the output power is nearly the same; thus, Class-B amplifiers have inherently lower gain than Class-A.

Another disadvantage of the Class-B amplifier is that is generates a high level of harmonics in the drain current by switching the FET on and off during each excitation cycle. If the device is terminated in the same impedance at the fundamental and second-harmonic frequencies, the second-harmonic output of an ideal Class-B amplifier is only 7.5 dB below the fundamental output (for reasons that will be examined in Section 9.3, the second-harmonic output of a practical amplifier is usually considerably lower). One solution to the problem of harmonics is to use a "push-pull" configuration, in which the excitation is applied out of phase to the inputs of two Class-B amplifiers and the outputs are combined out of phase. The phase shift of the output combiner must be 180 degrees at the harmonic frequencies as well as the fundamental frequency. This configuration, in conjunction with an appropriate design of the output matching network, can reduce significantly the levels of even harmonics.

In order to avoid the Class-B amplifier's inherently low gain and because the turn-off characteristic of power FETs are often very "soft," we rarely operate power FETs in a true Class-B mode. So-called Class-B microwave amplifiers are usually biased near $0.1I_{dss}$ and are actually operated in a mode somewhere between Class B and Class A. Conversely, Class-A amplifiers are often not operated in a classical Class-A mode: they