are sometimes biased to a minimal current level and driven well into saturation. Both types of operation are called *Class AB* and both represent a compromise between the extremes of either class: Class-AB amplifiers usually have better efficiency than Class-A amplifiers and better gain than Class-B amplifiers.

The requirements placed on microwave amplifiers tend to favor Class-A amplifiers over Class-B ones for most applications. Microwave amplifiers are usually used to amplify continuous signals of constant amplitude (e.g., frequency-modulated or phase-shift-keyed digital signals) in which the high quiescent power dissipation of the Class-A amplifier is not a significant problem. However, the gains of power MESFETs are often very low, especially compared to those of small-signal devices, so the gain advantage of the Class-A amplifier is significant. Although the theoretical dc-RF efficiency of the Class-B amplifier is attractive, the *power-added* efficiency, not the dc-RF efficiency, is usually more important.

Power-added efficiency is the ratio of the additional power provided by the amplifier to dc power; it is defined as

$$\eta_a = \frac{P_L - P_{\text{in}}}{P_{\text{dc}}} \tag{9.2.14}$$

where P_{in} is the RF input power. We can show easily that

$$\eta_a = \eta_{\text{dc}}\left(1 - \frac{1}{G_p}\right) \tag{9.2.15}$$

where G_p is the power gain; $G_p = P_L/P_{\text{in}}$. Equation (9.2.15) implies that the low gain of the Class-B amplifier somewhat offsets the advantage of high dc-RF efficiency: practical Class-B amplifiers usually have, at best, only slightly better power-added efficiency than Class-A amplifiers. Class-B amplifiers are most valuable for amplifying pulsed signals having low duty cycles, where their low average current requirements are a distinct advantage.

9.3 DESIGN OF MESFET POWER AMPLIFIER

In designing FET power amplifiers, we follow the general procedure used in the preceding three chapters: We employ the usual components of approximation and engineering judgement to generate an initial design, then optimize that design via numerical techniques. The numerical process we use to optimize the FET power amplifier is harmonic balance. Because

the Class-A amplifier is ideally a linear component, its initial design can employ linear circuit theory, usually very successfully. This is not the case with the Class-B amplifier, however, so we must be more careful with its design.

9.3.1 Approximate Design of Class-A FET Amplifiers

The first step in the design of a power amplifier is to select an appropriate MESFET. Most manufacturers of such devices know the output-power capabilities of their FETs, and this information is listed prominently on the specification sheets along with other traditionally optimistic claims. As a general rule, at frequencies below 12 GHz, most high-quality devices can produce output powers, as a function of gate width, of 0.3 W/mm at the 1-dB compression point and 0.5 W/mm when saturated. However, many experimental devices have produced power densities approaching 1 W/mm and many prosaic devices cannot achieve even 0.25 W/mm.

In designing the amplifier, we recognize that an ideal Class-A amplifier is, after all, a linear component. Therefore, although a practical Class-A amplifier is to some degree nonlinear, we should be able to rely fairly heavily on linear-amplifier theory in the initial approximate design. The fundamental problem in designing a Class-A amplifier, as in designing a small-signal linear amplifier, is to pick the appropriate source and load impedances: in a power amplifier, the load impedance must be selected to achieve the desired output power and the source impedance must provide a conjugate input match. Additionally, we must select a bias point that results in both adequate power and good efficiency.

We use the load-line approach described in Section 9.2 to select the real part of the load admittance. However, in order to select the load conductance properly, we must take into account the limits on the drain voltage and current as explained in Section 9.2. Figure 9.5 shows the terminal *I/V* characteristics of a power MESFET (i.e., with I_d expressed as a function of the terminal voltages V_{gs} and V_{ds} rather than as a function of the internal voltages V_g and V_d). We would prefer to have a plot of the internal *I/V* characteristics, the function $I_d(V_g, V_d)$, that does not include the voltage drops across the drain and source resistances. However, such curves are difficult to generate, and recognizing that this initial design is, after all, approximate, we shall accept a plot of the MESFET's terminal *I/V* characteristics as an approximation of the internal ones.

V_{min}, the minimum drain-source voltage, is limited to approximately 1.5 V by the knee of the *I/V* curve at $V_g = 0.6$ V; I_{max} is similarly limited. Because of a combination of effects, primarily the variation in V_t with V_d

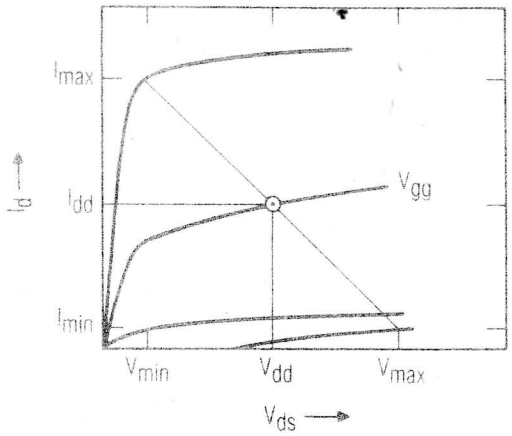


Figure 9.5 Drain *I/V* characteristics of a MESFET and the amplifier's load line. Because of the knee of the uppermost *I/V* characteristic, the minimum voltage is greater than zero. The optimum bias points are halfway between the maximum and minimum values of both voltage and current.

and the gate-drain avalanche limitation, V_d usually cannot be driven to the point where $I_d = 0$. Thus, there is a finite drain current, I_{min}, at V_{max}, the maximum value of V_d. V_{dd}, the dc drain-source voltage, is selected precisely halfway between V_{max} and V_{min}; I_{dd}, the quiescent dc drain current, is halfway between I_{max} and I_{min}. The gate-bias voltage that establishes this bias point is read directly from the *I/V* curves. We draw the load line superimposed on the *I/V* curves so that it connects these points; the load conductance is equal to the slope of the load line:

$$G_L = \frac{V_{max} - V_{min}}{I_{max} - I_{min}} \tag{9.3.1}$$

When an unpackaged MESFET is biased in its saturation region, the dominant component of its output admittance is the drain-source capacitance, C_{ds}. Because we wish to present a real load of conductance G_L to the terminals of the controlled current source I_d, the susceptance of the load must resonate with C_{ds}. Thus, the initial estimate of the load admittance is

$$Y_L = G_L - j\omega C_{ds} \tag{9.3.2}$$

If a packaged FET is used, determining the load impedance is complicated somewhat by the presence of the package parasitics but the underlying principle, presenting a real conductance of value G_L to the terminals of the current source, is still the same.

Because the load impedance at the terminals of the current source is real, the ac part of the drain voltage, $V_d(t)$, (which equals the load voltage, $V_L(t)$) and the load current, $I_L(t) = -I_d(t)$ are in phase (again, we write $I_d[V_g(t), V_d(t)]$ as $I_d(t)$ for simplicity). The output power is their product:

$$P_L = \frac{1}{2}\left[\frac{1}{2}(V_{max} - V_{min})\right]\left[\frac{1}{2}(I_{max} - I_{min})\right] \tag{9.3.3}$$

Some of this power is dissipated in the drain and source resistances, so for this reason as well as the others discussed in Section 9.2, (9.3.3) represents a slightly optimistic estimate. In a well designed MESFET, the power loss in these resistances is less than 1 dB.

The drain current of a Class-A amplifier should remain constant at the dc value under all excitation levels up to approximately the 1-dB gain compression point. As the amplifier is driven further into saturation, the $I_d(t)$ waveform becomes distorted and its average current changes. Below the compression point, the dc power equals the product of V_{dd} and I_{dd}; above the compression point, the dc power is usually greater but much of it is converted to RF output power. Therefore, the quiescent dc power can be considered an upper limit to the power dissipated by the device. If the amplifier has high gain and is to be operated only under excitation, the power dissipated by the device is approximately the difference between the output power and dc power. Designating the power dissipation P_d and the thermal resistance of the device from the channel to the mounting surface θ_{jc}, we find the temperature of the channel, T_{ch} to be

$$T_{ch} = T_a + P_d\theta_{jc} \tag{9.3.4}$$

where T_a is the temperature of the mounting surface. Equation (9.3.4) presupposes that the junction between the device and the mounting surface is thermally perfect; flaws in that junction, such as solder voids, can change the thermal resistance significantly or can cause "hot spots" on the surface of a large chip.

The input of the power FET amplifier is designed to be conjugately matched; therefore, we need to know the input impedance of the terminated MESFET. We can determine this impedance by using small-signal

S parameters and (8.1.5) and by repeating the calculation at appropriate intervals across the frequency range of interest. Finally, the small-signal gain can be found from (8.1.21) and stability factors and circles can be found from the appropriate equations, (8.1.2) and (8.1.7) through (8.1.10); the load impedance that optimizes output power is usually well within the stable region. Harmonic-balance analyses show that the input impedance varies only slightly with power level up to the point where the MESFET's gate begins to rectify the input signal significantly. Furthermore, in a well-designed amplifier, a good margin of small-signal stability is usually adequate to guarantee large-signal stability.

After the source and load impedances are determined, the matching networks can be designed. Designing the matching network is complicated by the fact that the source and load impedances are usually very low and it is best to short-circuit the drain at the harmonics of the excitation frequency. The latter requirement is not very severe in the case of Class-A amplifiers because the second and higher harmonic currents are not very great, but we shall see that it is very important in Class-B amplifiers. However, the combination of low impedances and high current densities requires careful consideration. The gate and drain currents in a power amplifier can be on the order of a few amperes, so even very small resistances can cause significant power dissipation. Capacitors, even those used for such prosaic purposes as dc blocking, must have high Qs, and inductors should not be made from narrow microstrips or fine wire (gold ribbon is a good material for inductors that must carry high currents). The topology of the matching circuit can often be selected to minimize the currents in components with relatively high loss.

We can estimate the source and load impedances at harmonics of the excitation frequency by analyzing the matching circuit via a general-purpose computer program for microwave circuit analysis. At high frequencies, the accuracy of such calculations deteriorates because of transmission-line discontinuities and the presence of high-order modes; however, at the same time, the large capacitances in the MESFET tend to short-circuit the external harmonic terminations and it becomes less important to terminate these harmonics accurately. With care, the matching circuits can usually be analyzed to obtain reasonable estimates of embedding impedances at frequencies as high as 18–20 GHz.

The final step in the design process is to check the circuit via a harmonic-balance analysis. The primary purposes of this step are to ascertain that the required output power will be achieved, to determine the harmonic output power and the degree of saturation, and to time-tune the bias voltages and load and source impedances to optimize the performance.

If the approximate design has been performed carefully, the harmonic-balance analysis will probably indicate that the approximate design is not far from the optimum.

9.3.2 Approximate Design of Class-B FET Amplifiers

The design of the Class-B amplifier parallels that of the Class-A amplifier. The load impedance of an ideal Class-B amplifier is the same as that of an ideal Class-A amplifier having the same output power, and we find from harmonic-balance analyses that a real MESFET's optimum Class-B and Class-A load impedances are often identical. In general, however, it is not possible to estimate the linear gain or input impedance of a Class-B amplifier from small-signal S parameters; instead, we use the MESFET's circuit model to estimate the input impedance and the harmonic-balance analysis to determine gain.

The maximum value of V_d allowable in a Class-B amplifier is somewhat lower than that of a Class-A amplifier. In FET amplifiers that are limited by gate-drain avalanching, the output power in Class-B operation is lower than that in Class-A operation. However, if the amplifiers are not limited by avalanche breakdown, the output powers of both classes are nearly identical. Thus, we can use the same procedure to select the load impedance of a Class-B amplifier as is used for a Class-A amplifier, as long as $V_{\max}$ is chosen to have its Class-B value.

The dc drain current of a Class-A amplifier under full excitation can be estimated as $I_{\max}/\pi$. The dc power dissipation is

$$P_d = V_{\text{dd}} \frac{I_{\max}}{\pi} \tag{9.3.5}$$

This estimate of the dc drain current is reasonable at the 1-dB saturation point; however, because the drain current varies with drive level, it is not valid at other levels. Furthermore, because of the inherently low gain of the Class-B amplifier, the RF input power may be relatively high and therefore may contribute significantly to power dissipation. Equation (9.3.4) is a valid expression for the channel temperature of a Class-B amplifier as well as a Class-A amplifier.

In an ideal Class-A amplifier, the gate-source voltage V_g varies between V_t and the threshold of gate conduction, approximately 0.5 V. In a Class-B amplifier, V_g varies between $\approx 2V_t$ and the same maximum voltage. Therefore, in order to deliver the same output power, the Class-B amplifier

requires approximately twice the voltage across C_{gs} as the Class-A; accordingly, we might conclude that the Class-B input power must be 6 dB greater, so the gain must be 6 dB lower. This conclusion is troubling because many power MESFETS exhibit little more than 6 dB gain in Class-A operation. Fortunately, the situation is not quite that bad for several reasons: First, even in the ideal case, the difference in voltage is usually slightly less than a factor of two; second, the Class-B amplifier is often biased slightly above V_t, so it has a small quiescent drain current, which reduces the difference in the variation of V_g even further; and third, because the gate-bias voltage is more negative, C_{gs} is lower in Class B than in Class A. As a result, the difference in gain between Class-B and Class-A amplifiers using the same FET is usually from 3 to 5 dB, still significant but not as disastrous as 6 dB.

An adequate initial estimate of the input impedance of the Class-B amplifier is:

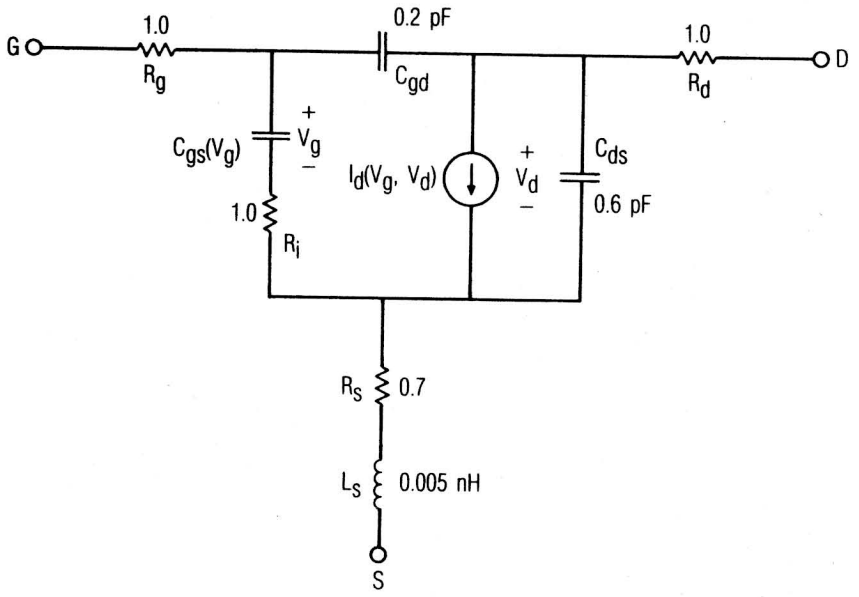
$$Z_{in} = R_g + R_i + R_s + \frac{\langle g_m \rangle L_s}{C_{gs}(V_t)} + j\left[\omega L_s - \frac{1}{\omega C_{gs}(V_t)}\right] \qquad (9.3.6)$$

that is, the sum of the impedances in the input loop of the MESFET. The term $\langle g_m \rangle$ is the transconductance averaged over the excitation cycle; $\langle g_m \rangle \approx 20$ percent of the peak transconductance. This impedance can be calculated more precisely by the harmonic-balance analysis; like that of the Class-A amplifier, the input impedance of the Class-B amplifier is not unduly sensitive to RF input level as long as the FET is not driven to the point where the gate junction rectifies the input signal.

9.3.3 Design Examples and Performance Study

To further investigate the design and performance of FET power amplifiers, we shall design Class-A and Class-B amplifiers using a common MESFET and optimize the design via harmonic-balance analysis. Although we shall see that the approximate design procedure is remarkably good when applied to Class-A amplifiers, it is not quite as reliable when applied to Class-B amplifiers, and in neither case does it produce all the information we would like to have with adequate accuracy.

The device we shall use is an experimental X-band power MESFET that has a gate width of 2.4 mm and an output power capability of slightly less than 1 W. The amplifier will be operated at 10 GHz. The equivalent circuit of the MESFET is shown in Figure 9.6(a), and its *I/V* characteristics are shown in Figure 9.6(b). We model the gate-source capacitance as an ideal uniformly doped Schottky barrier having a zero-voltage capacitance



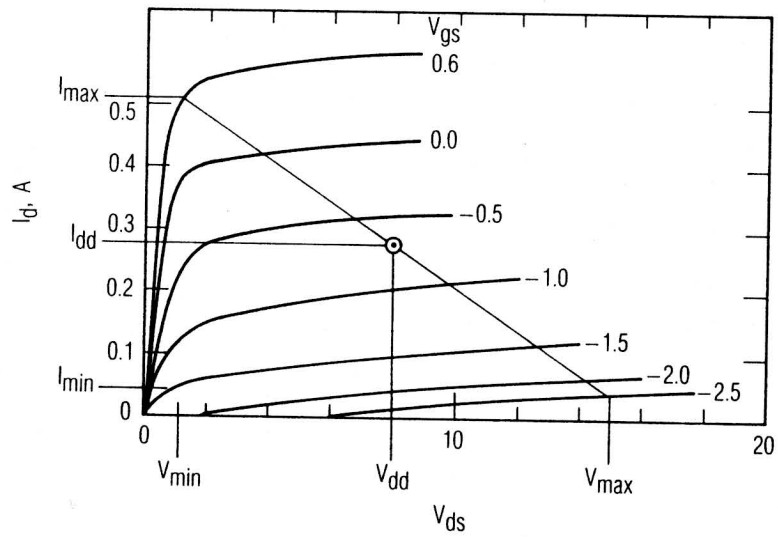


Figure 9.6 (a) Equivalent circuit of the 2.4-mm power MESFET used in the design examples; (b) the MESFET's *I/V* characteristics, including the load line.

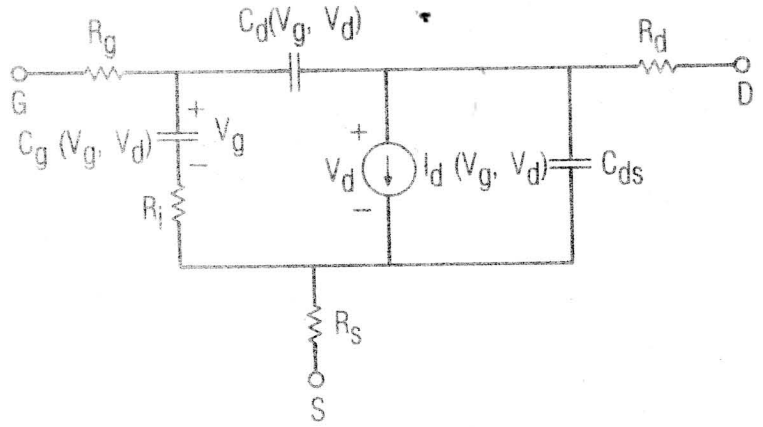


Figure 2.16 GaAs MESFET nonlinear equivalent circuit.

$$C_g(V_g, V_d) = \left.\frac{\partial Q_d}{\partial V_g}\right|_{V_d - V_g = \text{constant}} \tag{2.4.1}$$

$$C_d(V_g, V_d) = \left.\frac{\partial Q_d}{\partial V_d}\right|_{V_g = \text{constant}} \tag{2.4.2}$$

where Q_d is the charge in the gate depletion region. Unlike the small-signal incremental characterization of (2.2.21), this formulation is valid for large-signal operation; it gives the current in C_g and C_d, respectively, as

$$I_{Cg} = \frac{\partial Q_d}{\partial V_g}\frac{dV_g}{dt} = C_g(V_g, V_d)\frac{dV_g}{dt} \tag{2.4.3}$$

$$I_{Cd} = \frac{\partial Q_d}{\partial V_d}\frac{dV_f}{dt} = C_d(V_g, V_d)\frac{dV_f}{dt} \tag{2.4.4}$$

where V_f is the voltage across C_d.

Examples of the voltage dependence of C_g and C_d are shown in Figure 2.17. If the FET is in saturation, C_g can usually be modeled with good accuracy as a Schottky-barrier capacitance; however, the C/V characteristic may deviate significantly from (2.3.5) when the reverse gate voltage exceeds V_t and the channel is fully depleted. At that point, the change in Q_d with gate voltage is significantly reduced, so C_g drops rapidly. C_d can

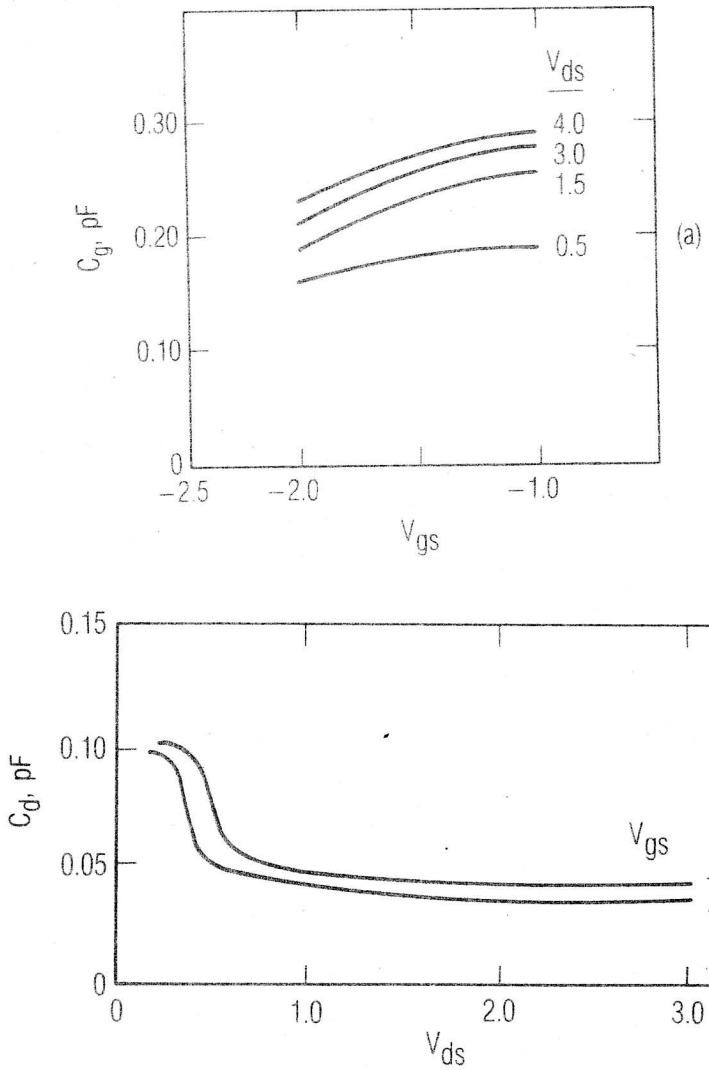


Figure 2.17 (a) Measured gate-source capacitance and (b) gate-drain capacitance of a commercial 0.5μ × 300μ MESFET.

be assumed to be constant as long as the FET remains in its saturation region, as it usually does in most well designed nonlinear or quasilinear components. In saturation, the capacitance between the gate and drain