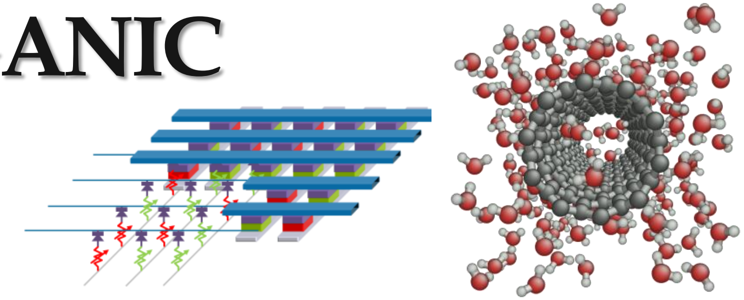
NON-VOLATILE MEMORY DEVICES: FROM SILICON TO ORGANIC MATERIALS



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Lecture for the course «Tecnologie e dispositivi elettronici avanzati»

April 6th, 2017

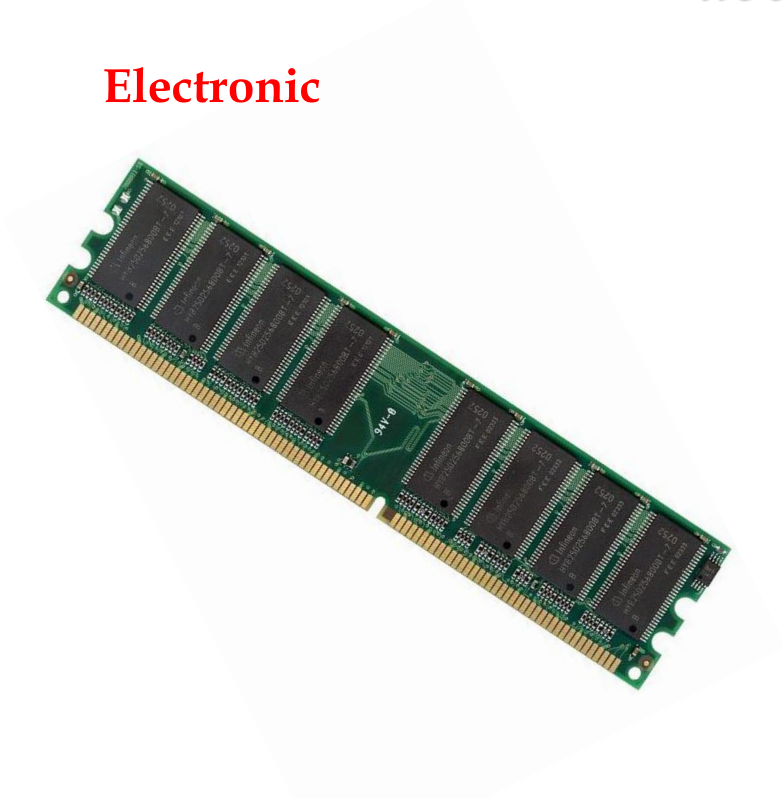
Outline

- Introduction: memory concept and classification
- Conventional memory technologies
- Emerging memory technologies: from inorganic to organic electronics
- Potential and challenges of organic memory devices
- Organic memory structures
- Organic Transistor-type memories
- Organic Resistor-type memories

What is an electronic memory?

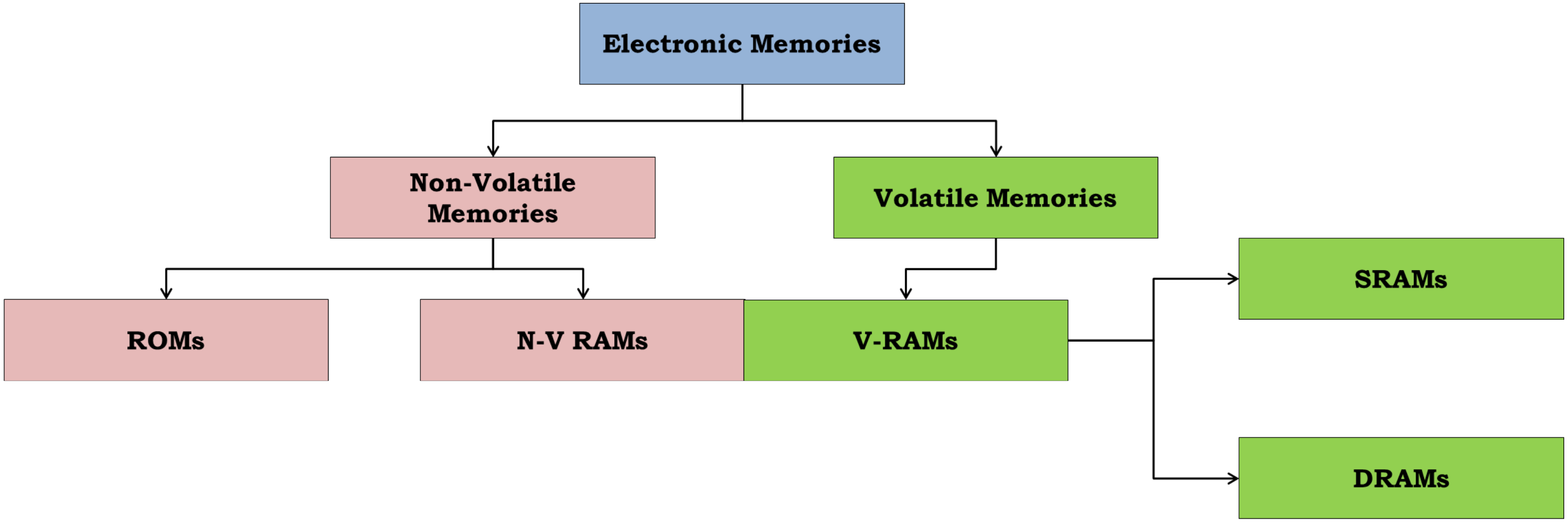
An electronic memory is a component, device or recording medium used to store data for retrieval on a termporary or permanent basis for use in a computer or other electronic devices

Electronic



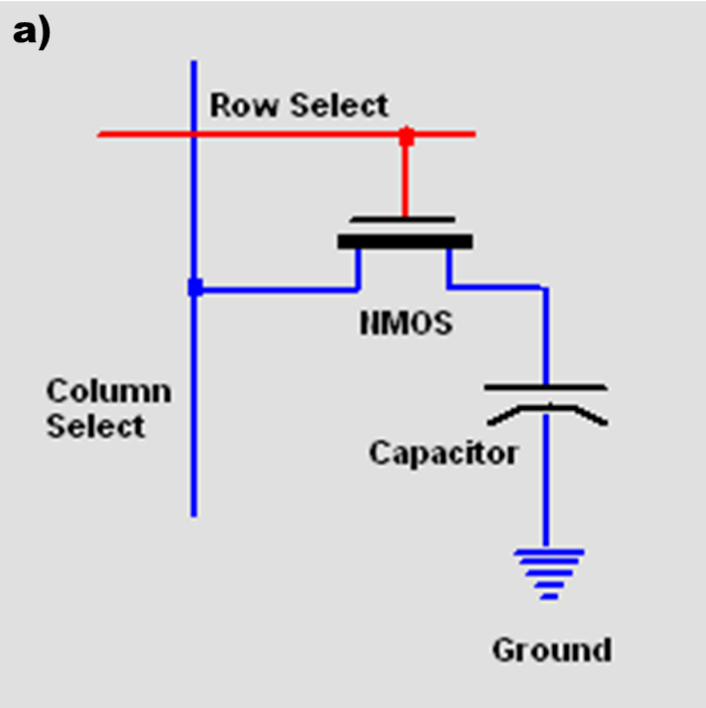
Mechanical (CD, DVD, Hard disk)

Classification of electronic memories



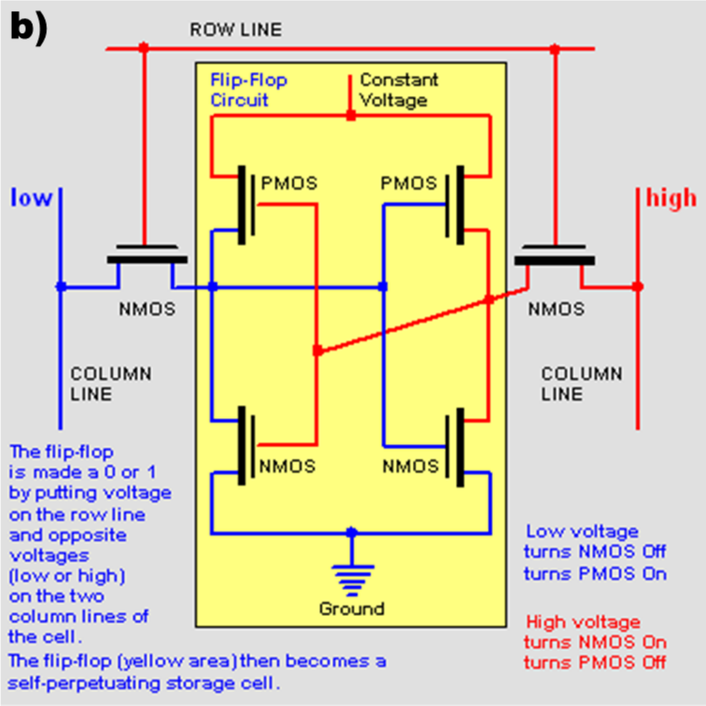
Classification of electronic memories

Advantages:
- Simple structure
- High density



DRAM: Dinamic RAM

Advantages:
- Low power consumption
- High speed



The flip-flop is made a 0 or 1 by putting voltage on the row line and opposite voltages (low or high) on the two column lines of the cell.

The flip-flop (yellow area) then becomes a self-perpetuating storage cell.

Low voltage turns NMOS Off turns PMOS On

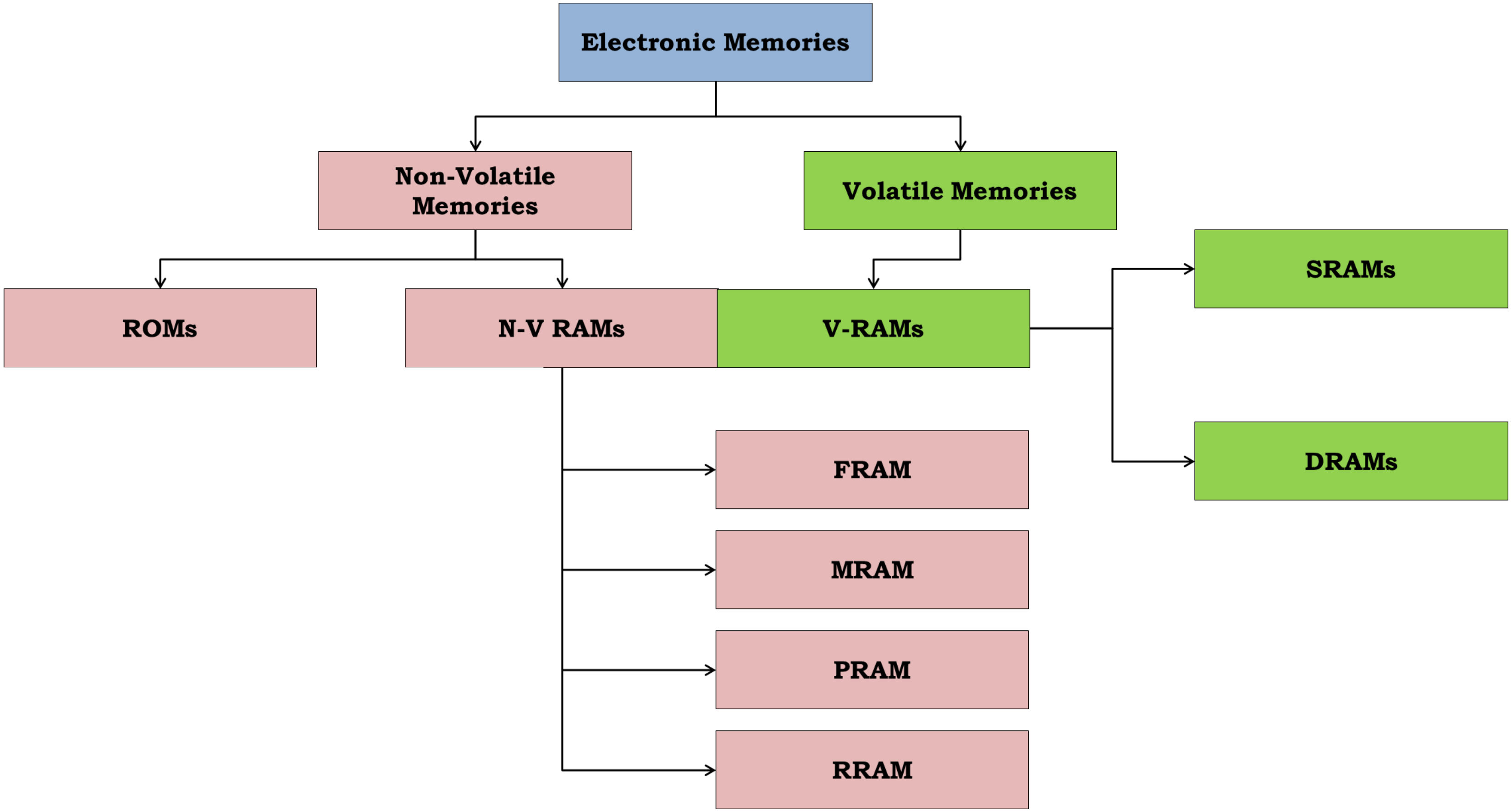
High voltage turns NMOS On turns PMOS Off

SRAM: Static RAM

→ **SRAMs**

→ **DRAMs**

Classification of electronic memories


Electronic Memories

Non-Volatile Memories

Volatile Memories

ROMs

N-V RAMs

V-RAMs

SRAMs

DRAMs

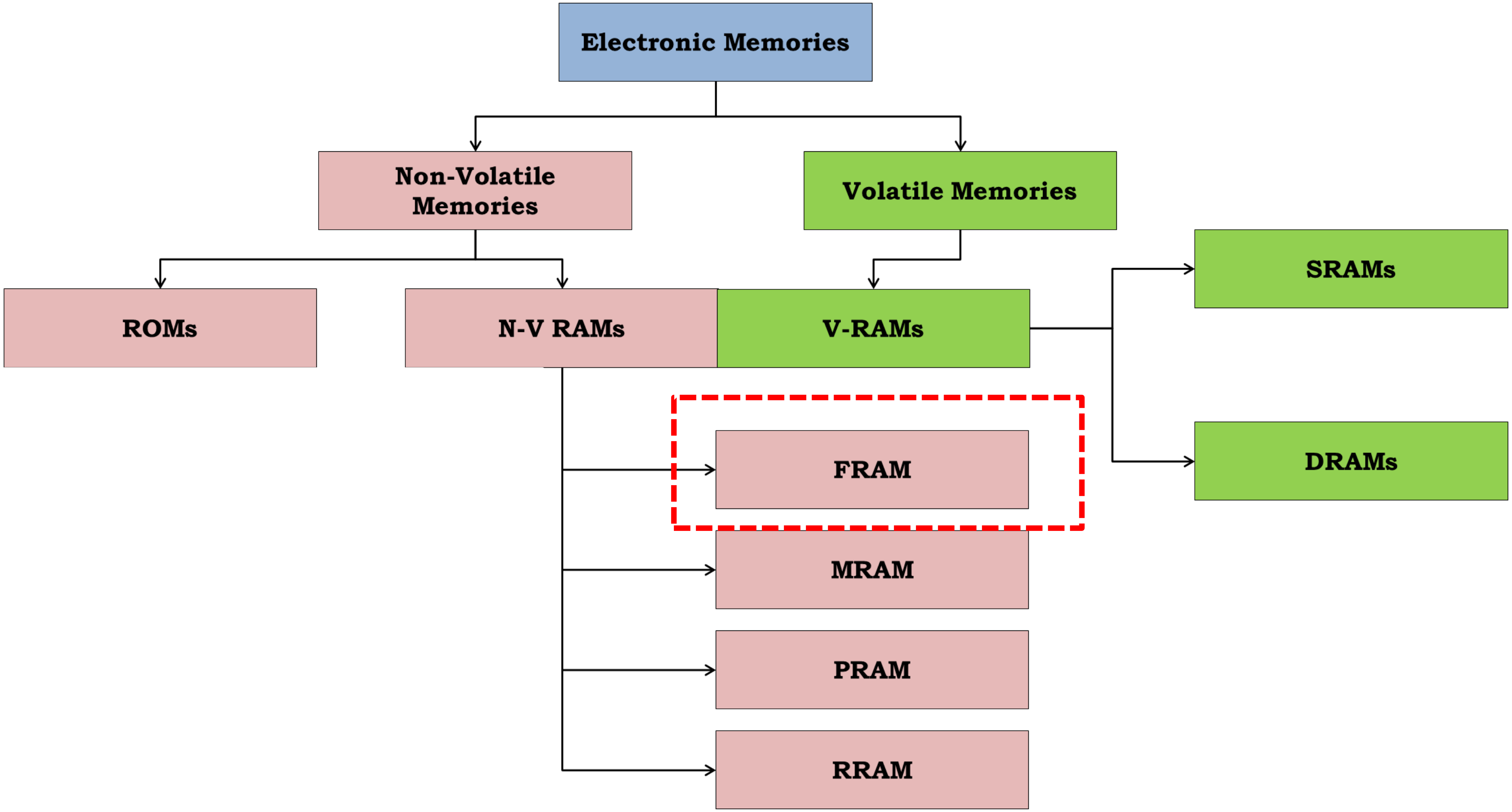
FRAM

MRAM

PRAM

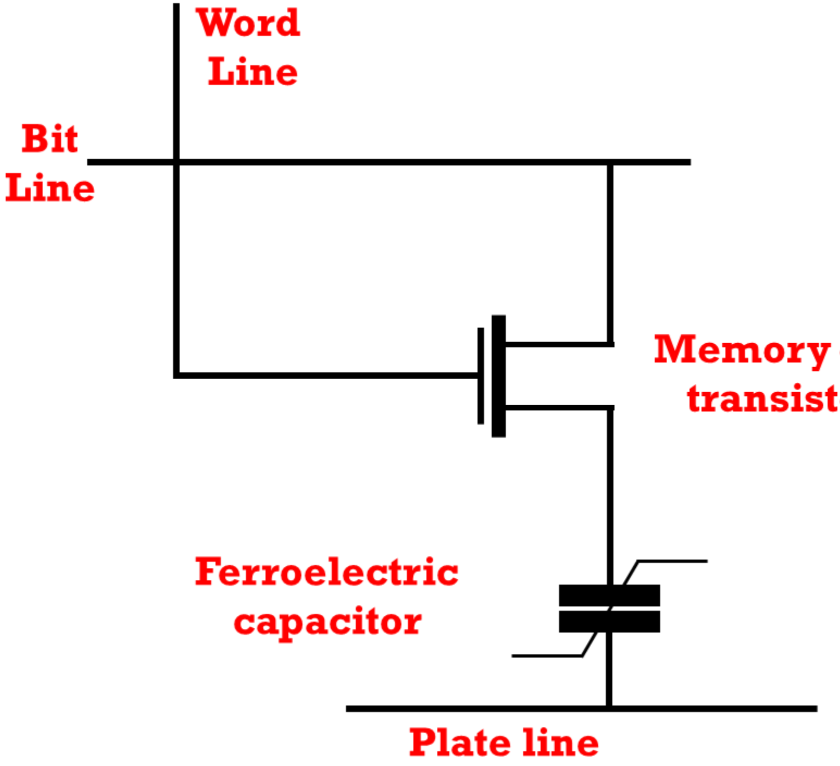
RRAM

Classification of electronic memories



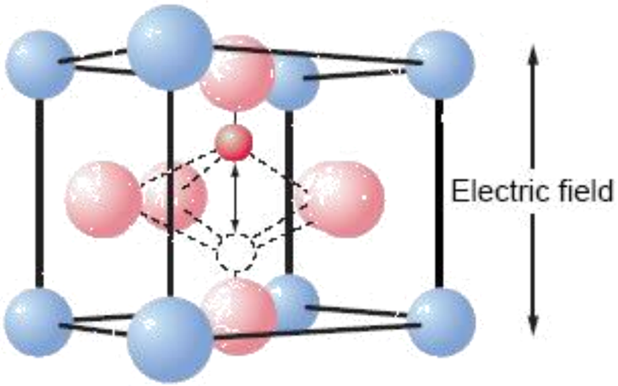
Classification of electronic memories

Ferroelectric RAM (FRAM)



What are ferroelectric materials??

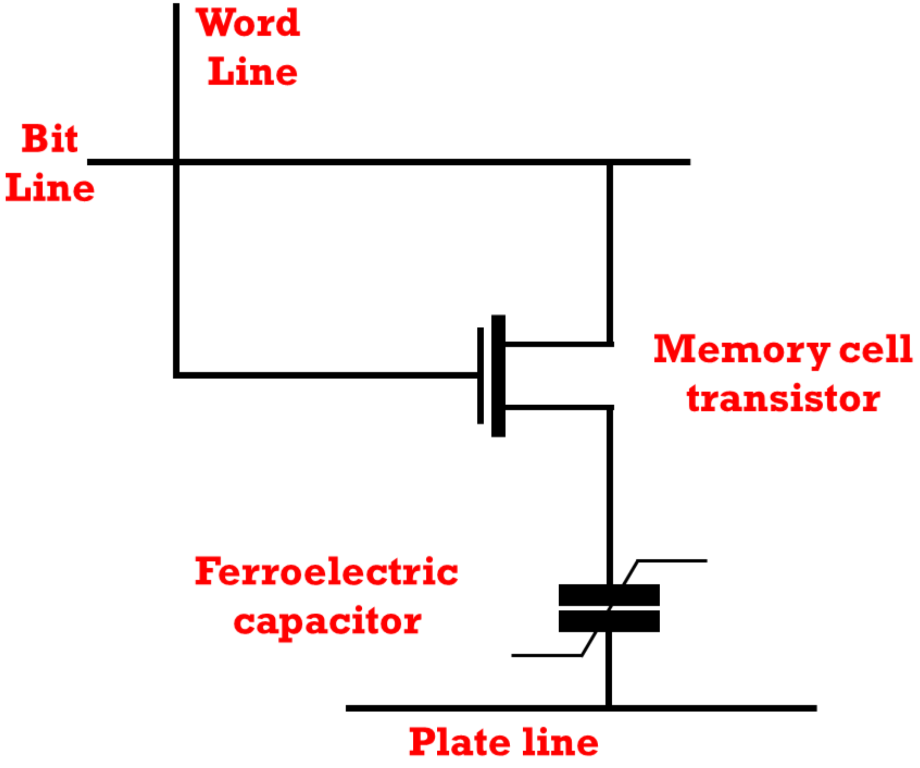
Materials composed of crystals in which the structural units are tiny electric dipoles

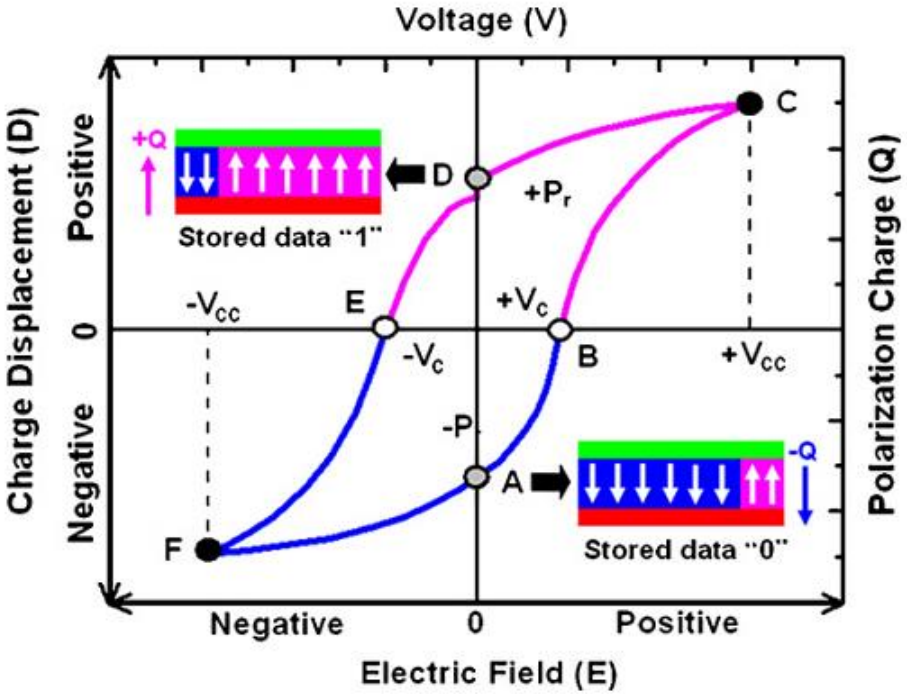


- Use electric field and ferroelectric effects to store data
- Exploit a ferroelectric capacitor
- Introduce in the late 1980s

Classification of electronic memories

Ferroelectric RAM (FRAM)





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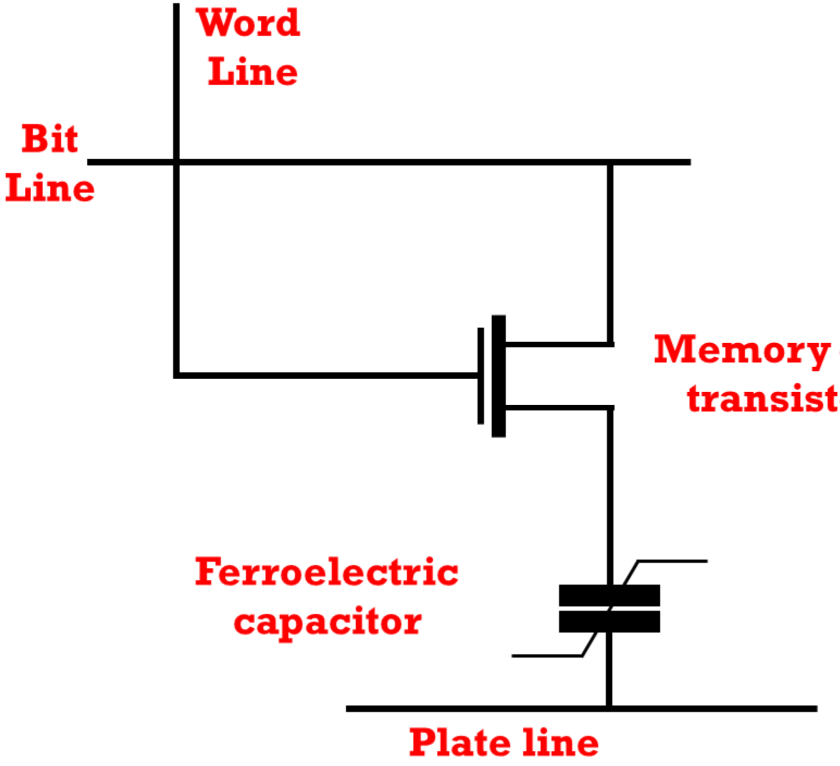
Classification of electronic memories

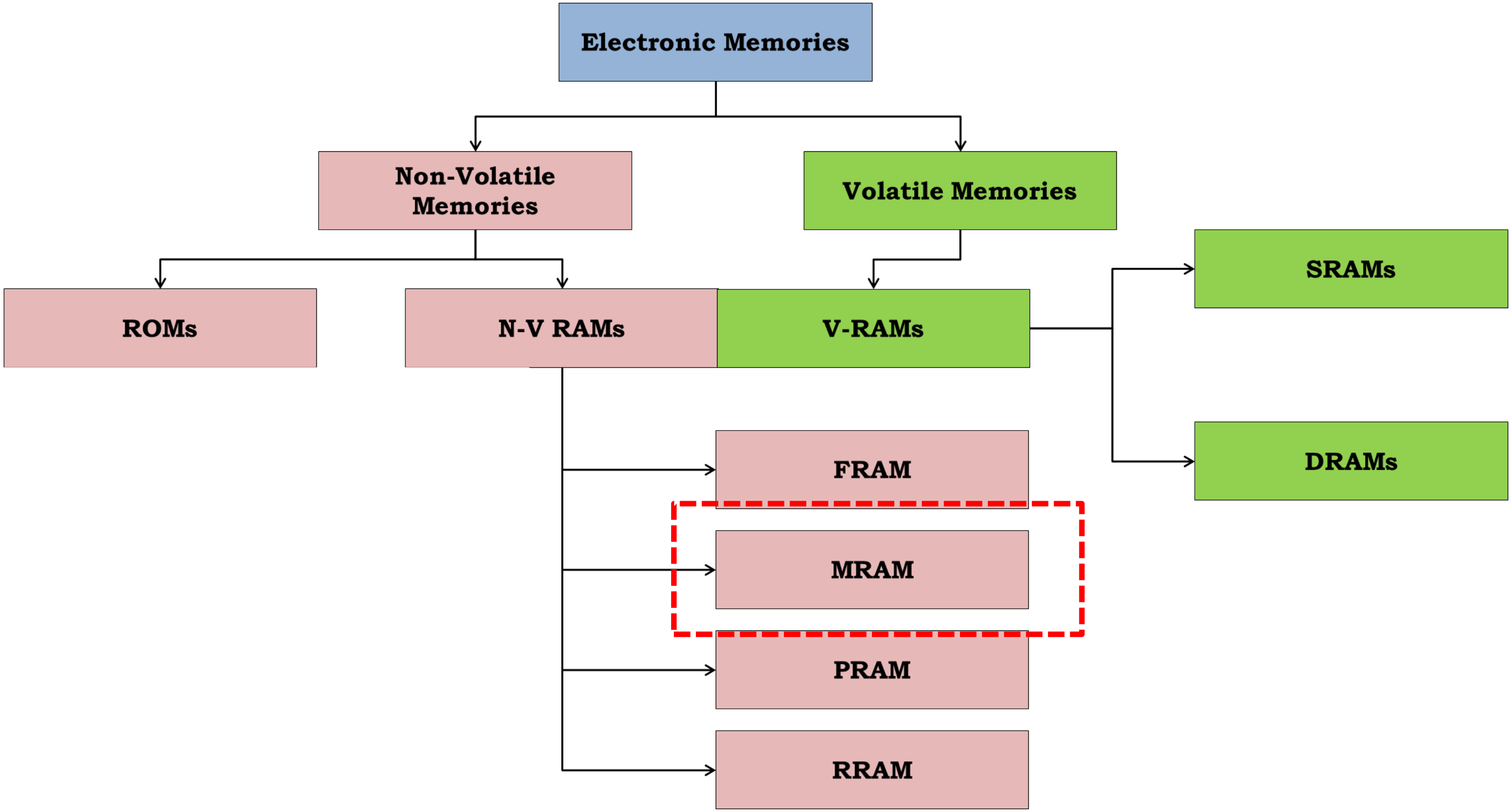
Ferroelectric RAM (FRAM)



Advantages:
- Low power consumption
- Fast write speed
- Good cyclability

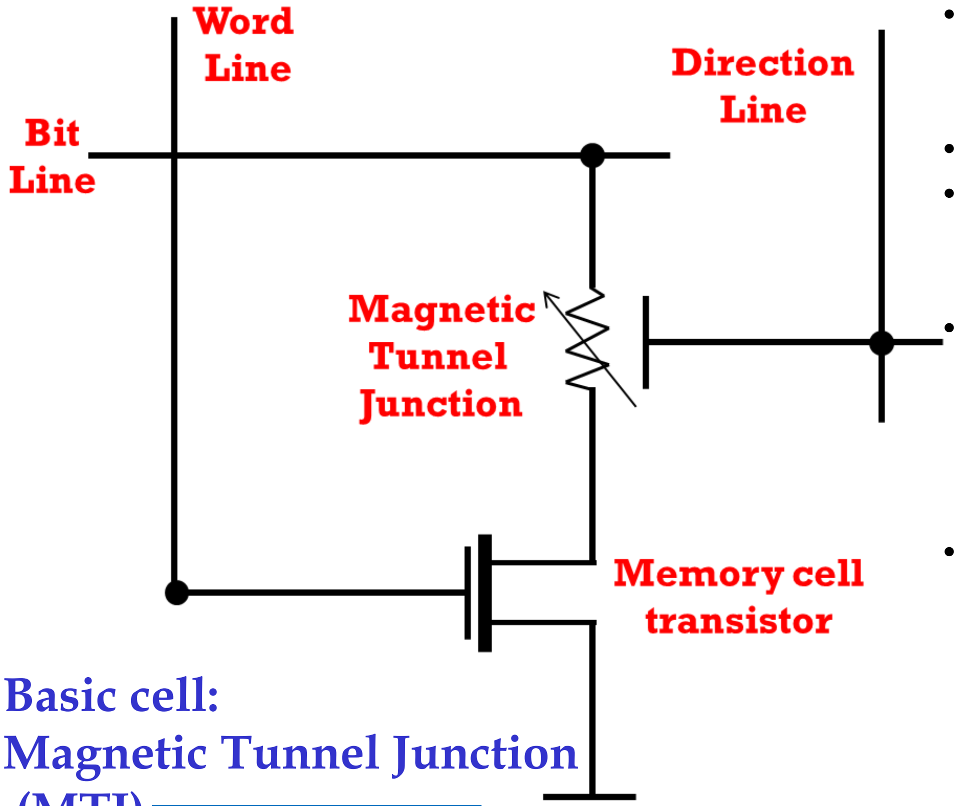
- Use electric field and ferroelectric effects to store data
- Exploit a ferroelectric capacitor
- Introduce in the late 1980s

Classification of electronic memories

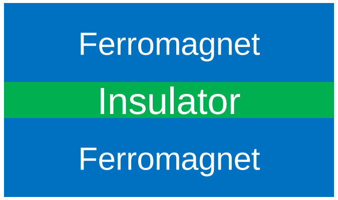


Classification of electronic memories

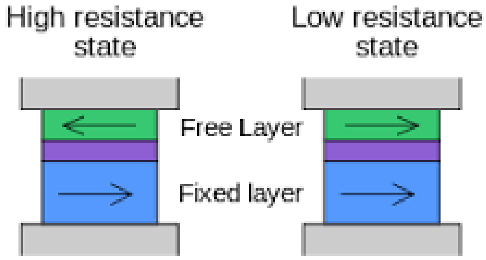
Magnetic RAM (MRAM)



Basic cell: Magnetic Tunnel Junction (MTJ)

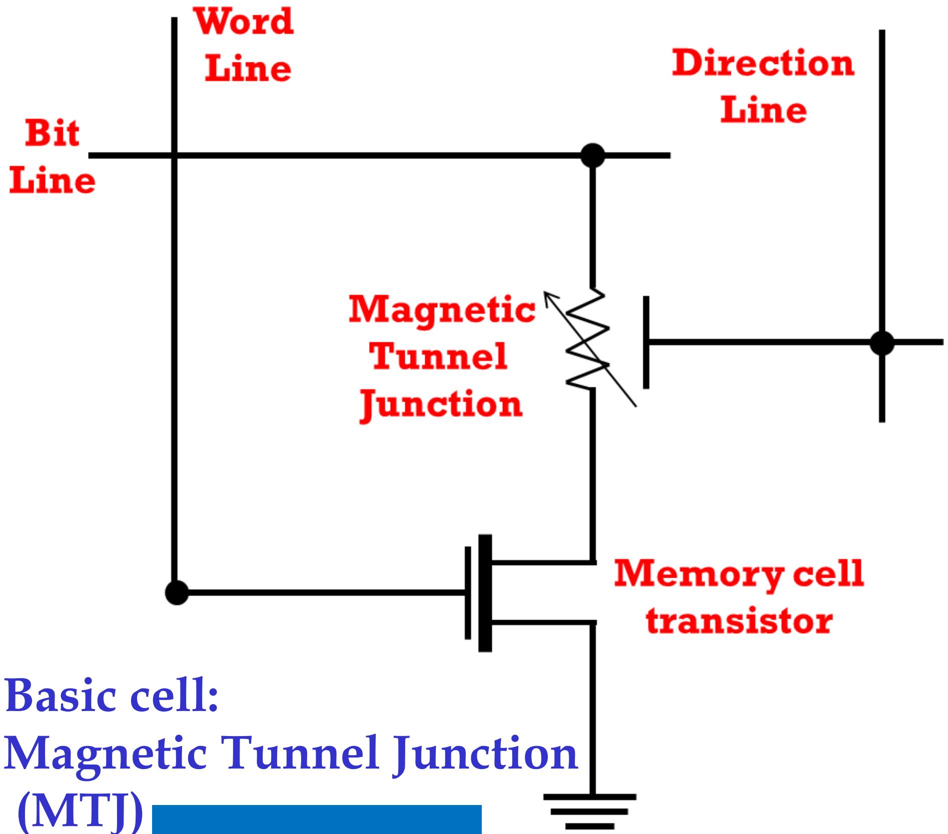


- Each MTJ is composed of **two layers** (**ferromagnetic** plates), fixed and free, separated by a **thin dielectric material**
- **Fixed** layer : Magnetic polarity is fixed
- **Free** Layer : Magnetic polarity is subject to change in accordance with the magnetic field which is the resultant of the applied current
- The MTJ device has a **low resistance** when the magnetic moment of the free layer is **parallel** to the fixed layer and a **high resistance** when the free layer moment is oriented **anti-parallel** to the fixed layer moment.
- The **data** is **stored** as a **magnetic state** rather than a charge, and sensed by measuring the resistance without disturbing the magnetic state

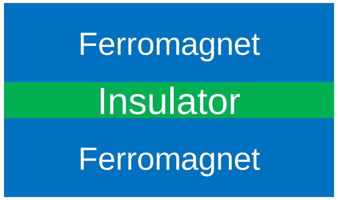


Classification of electronic memories

Magnetic RAM (MRAM)



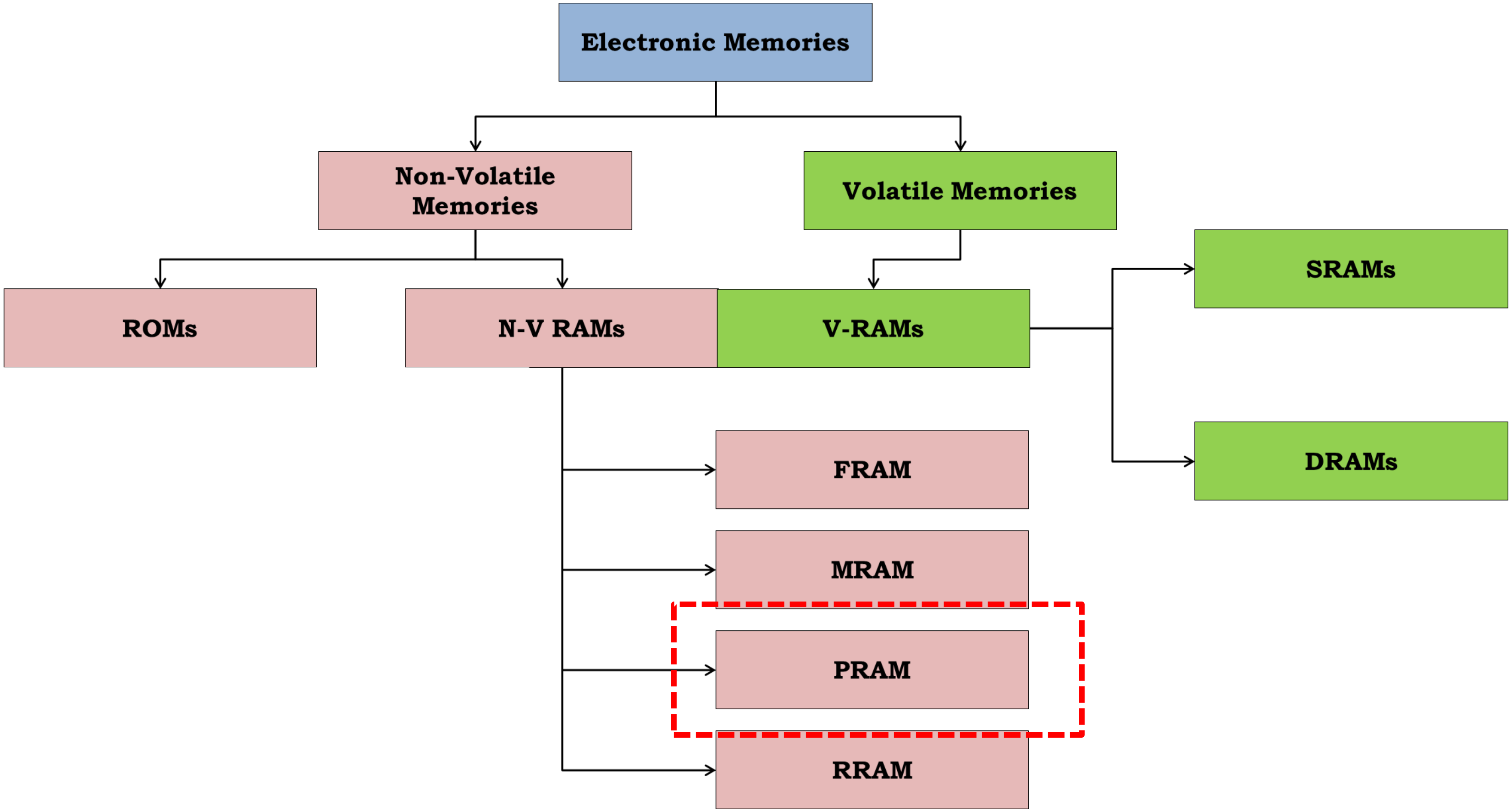
Basic cell:
Magnetic Tunnel Junction (MTJ)


Ferromagnet
Insulator
Ferromagnet

Advantages:

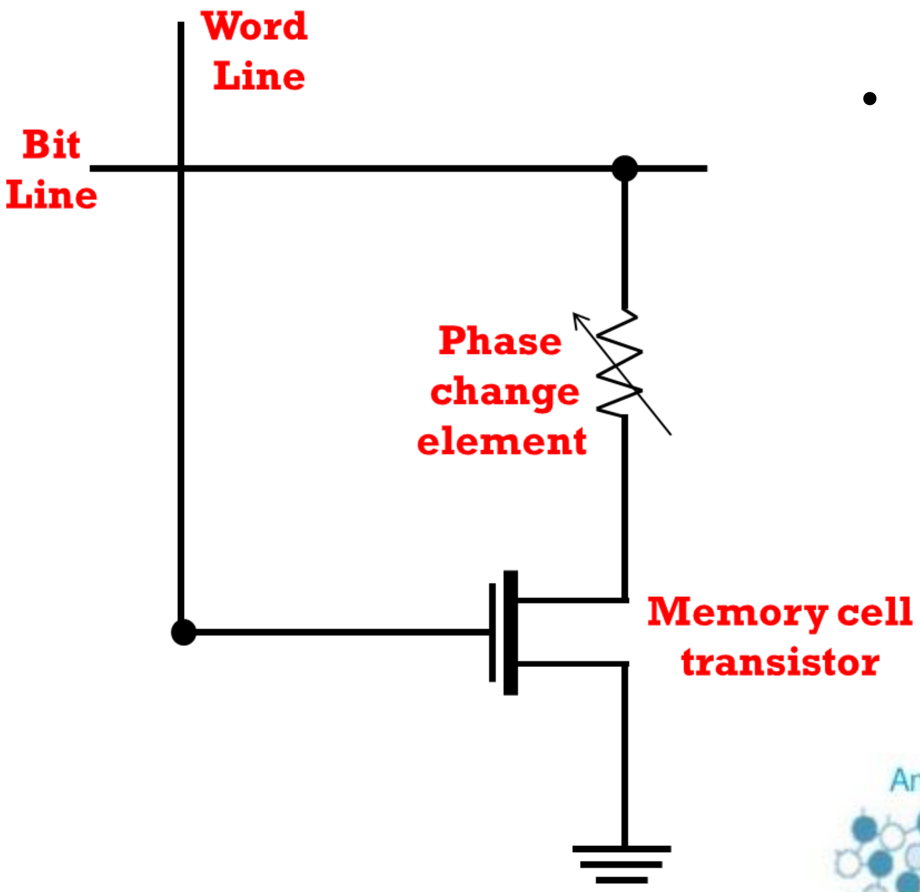
- Lower power consumption than DRAM
- Density similar to DRAM
- Much faster than DRAM
- Suffer no degradetion over time

Classification of electronic memories



Classification of electronic memories

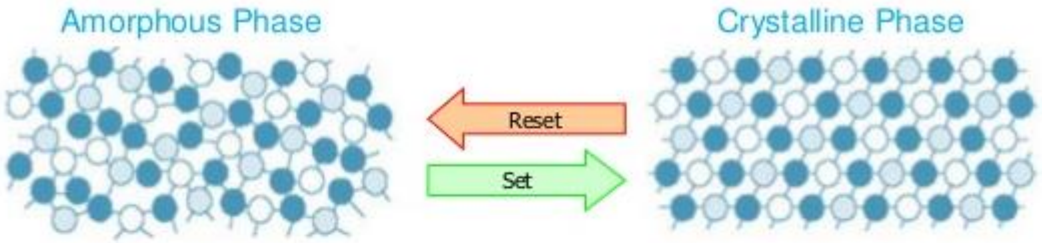
Phase-change RAM (PRAM)



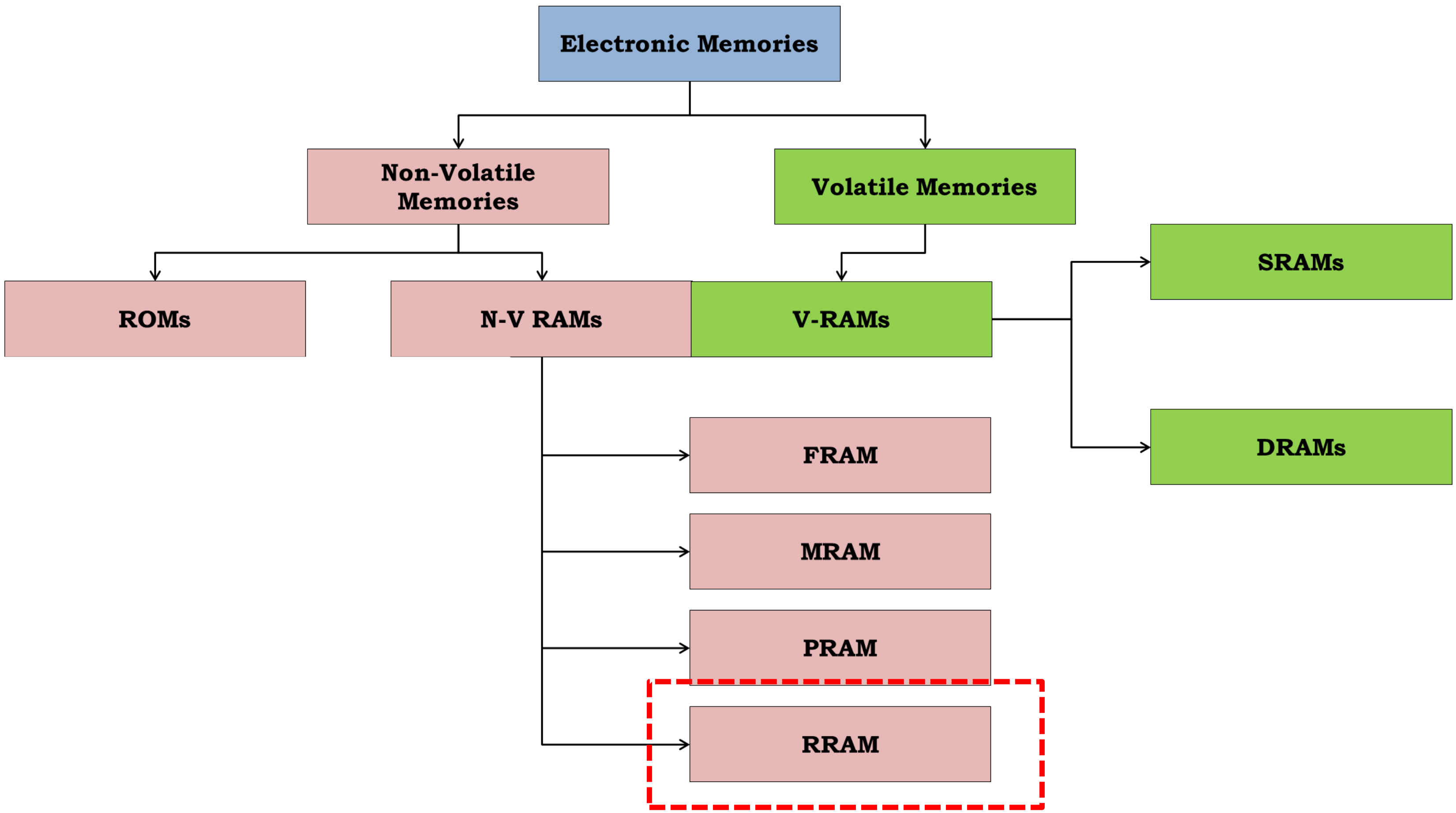
- Exploit the unique property of phase-change materials (chalcogenides): reversible phase transition between amorphous (high resistance state - logic 0) and crystalline phases (low resistance state - logic 1)

Advantages:

- **Inherent scalability**
- **Switching time**



Classification of electronic memories


Electronic Memories

Non-Volatile Memories

Volatile Memories

ROMs

N-V RAMs

V-RAMs

SRAMs

DRAMs

FRAM

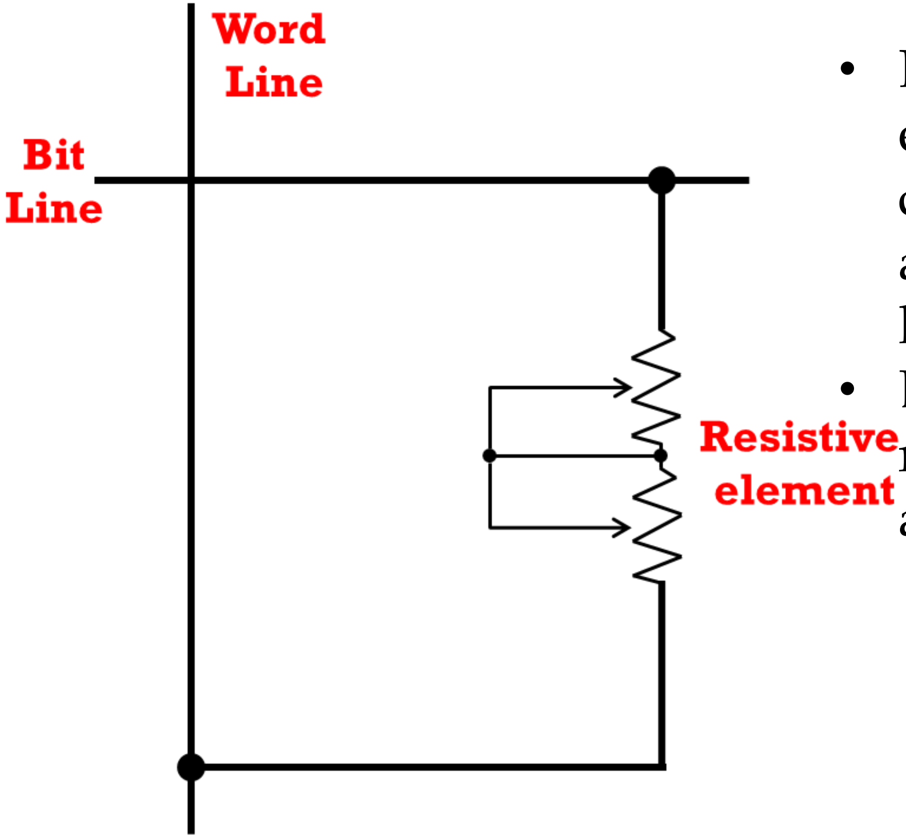
MRAM

PRAM

RRAM

Classification of electronic memories

Resistive RAM (RRAM)

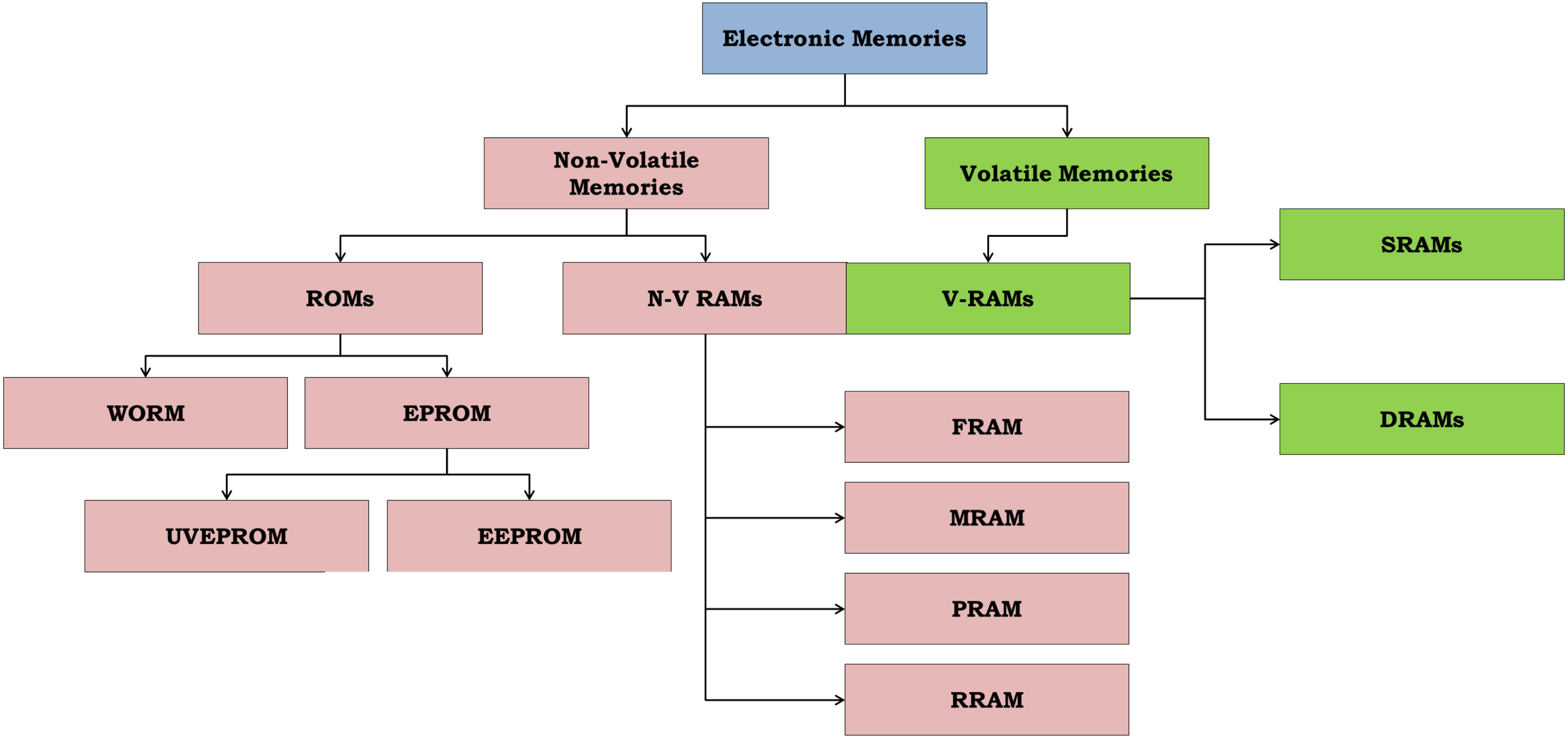


- Each cell consist of a top and a bottom electrode sandwiching a resistive layer, characterized by two resistance states: an high resistance state (HRS) and a low resistance state (LRS)
- By applying a voltage to the cell, resistive switching between the HRS and the LRS can be achieved

Advantages:

- **Simple and small structure**
- **No access transistors**
- **Integration in cross bar arrays**

Classification of electronic memories



Electronic Memories

Non-Volatile Memories

Volatile Memories

ROMs

N-V RAMs

V-RAMs

SRAMs

DRAMs

WORM

EPROM

UVEPROM

EEPROM

FRAM

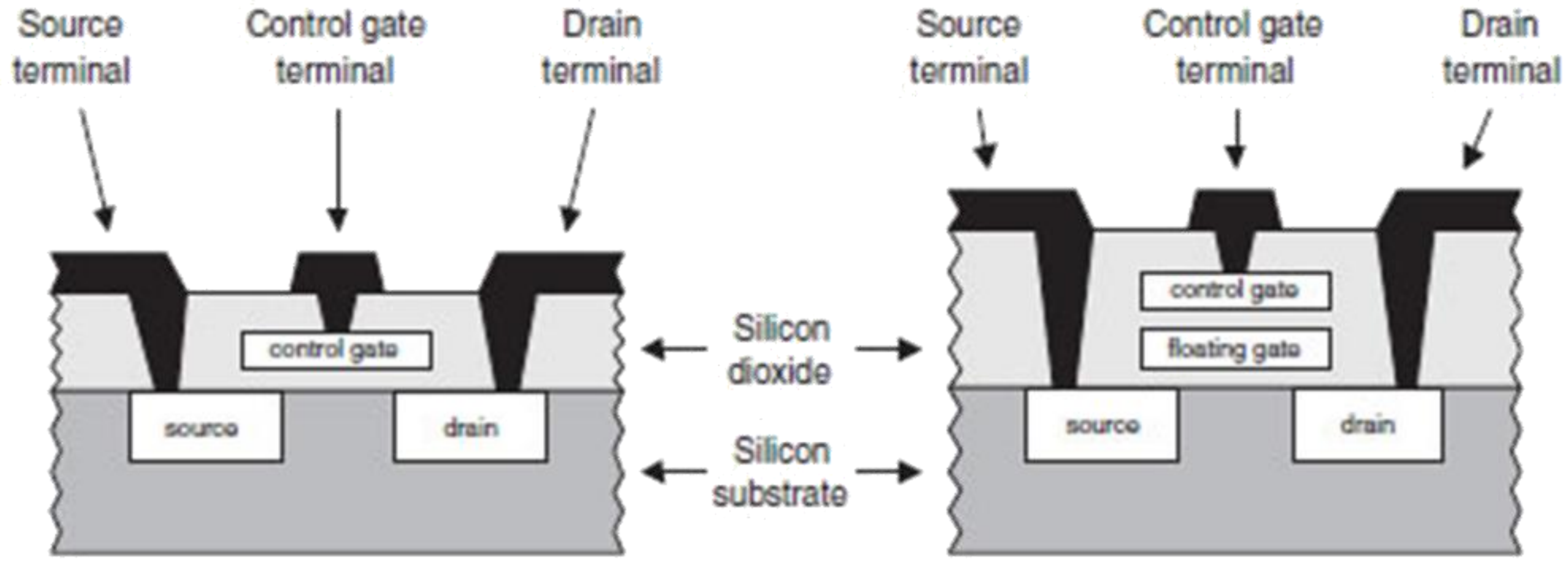
MRAM

PRAM

RRAM

Classification of electronic memories

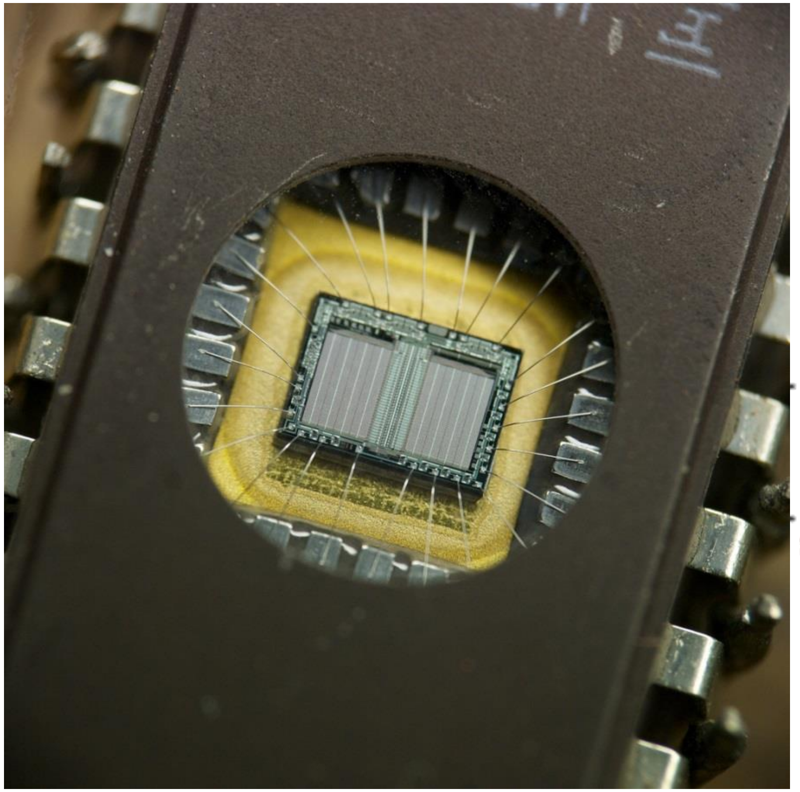
UVEPROM

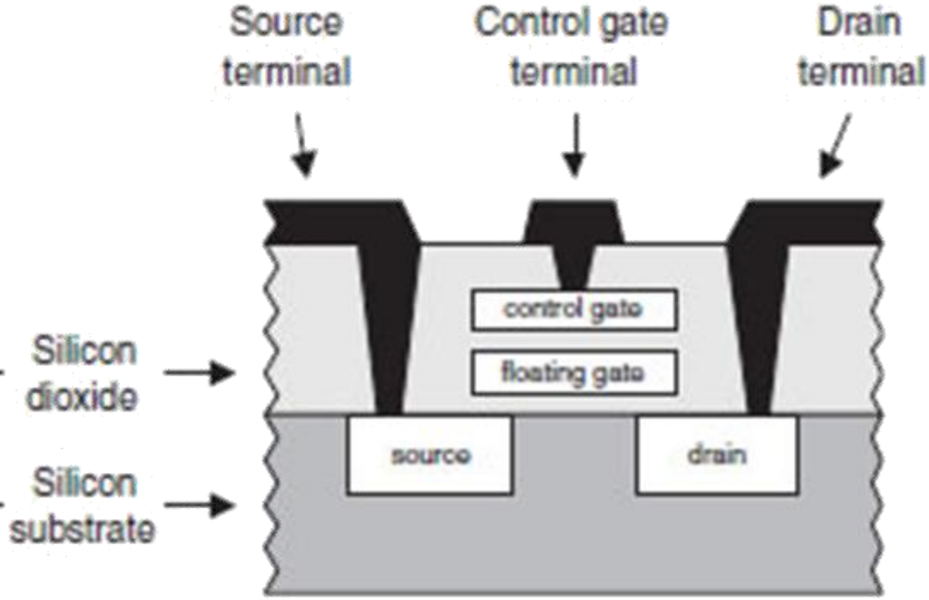


a) Standard MOS transistor b) UVEPROM transistor

Classification of electronic memories

UVEPROM



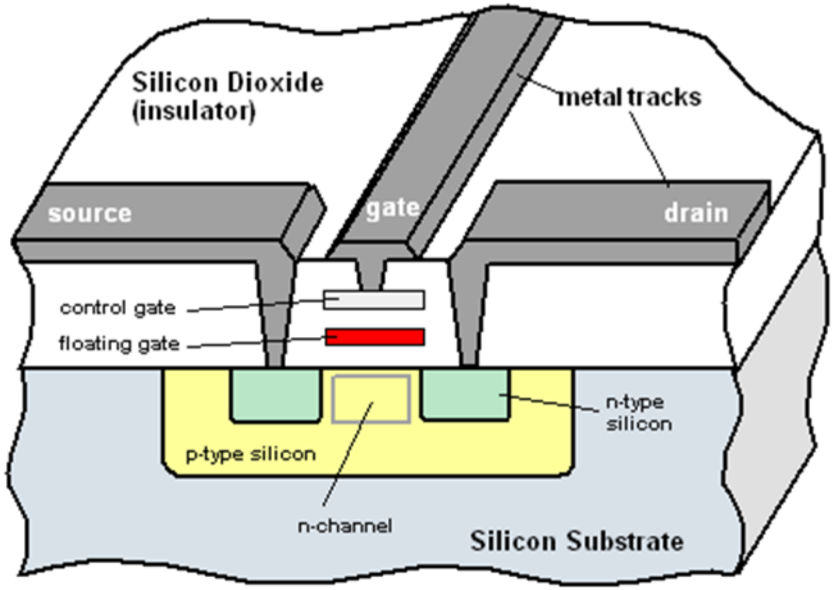


b) UVEPROM transistor

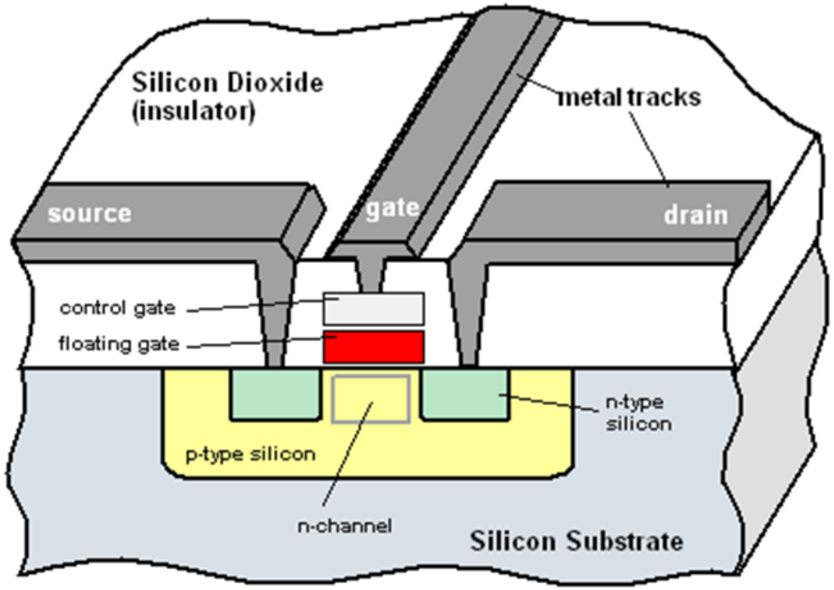
Classification of electronic memories

EEPROM

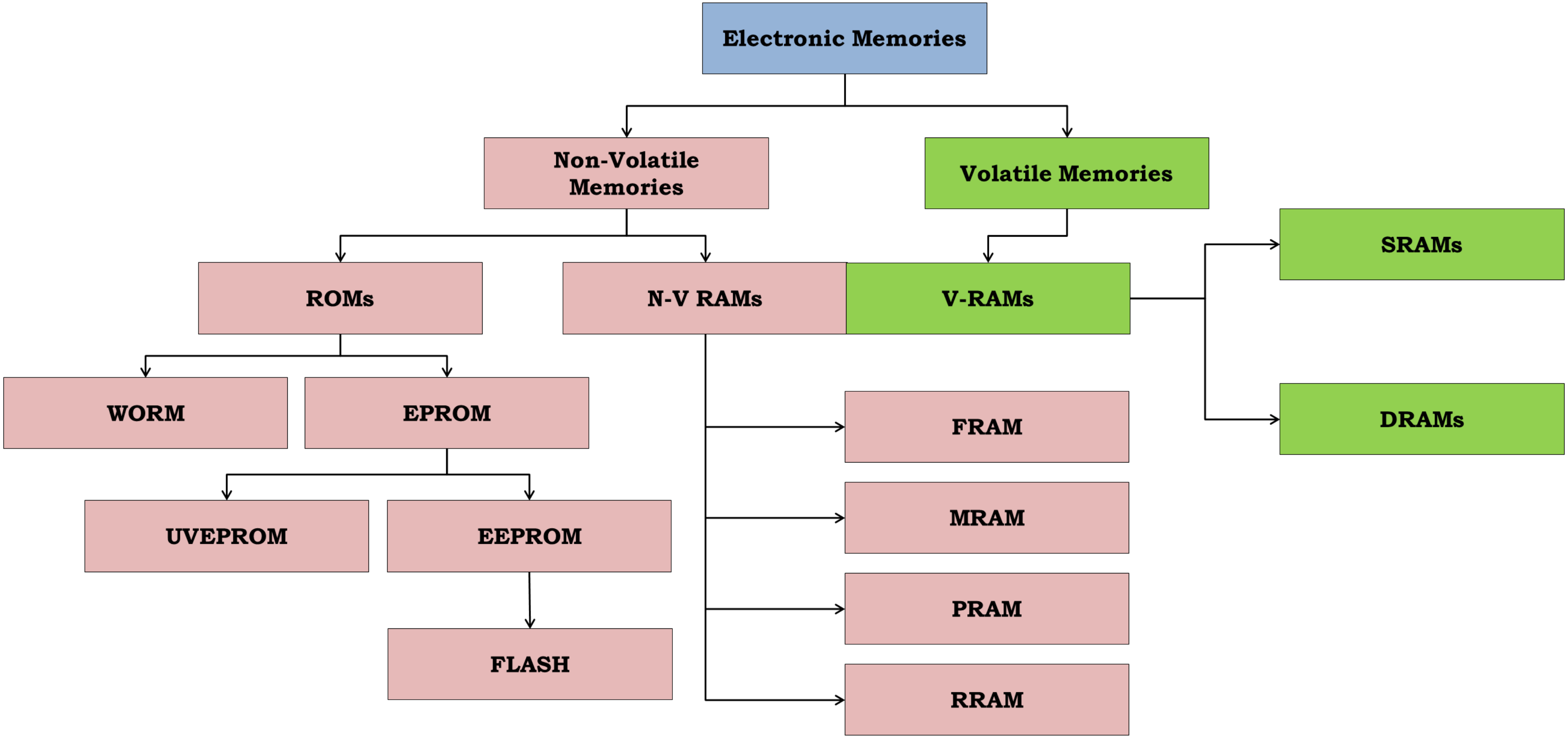
a) UVEPROM transistor



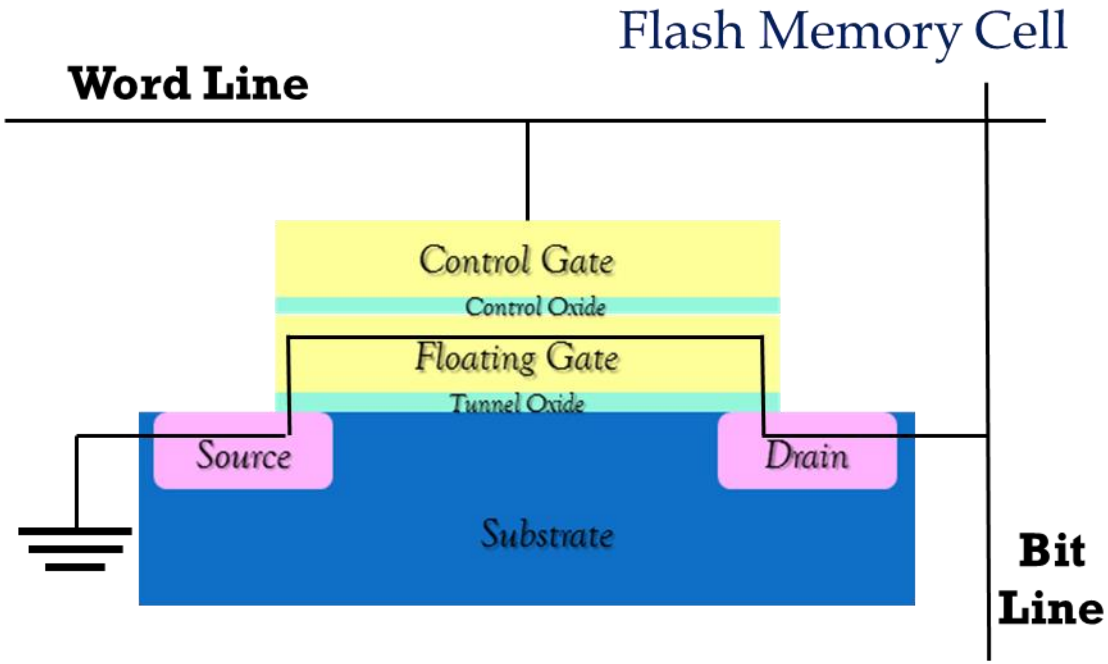
b) EEPROM transistor



Classification of electronic memories



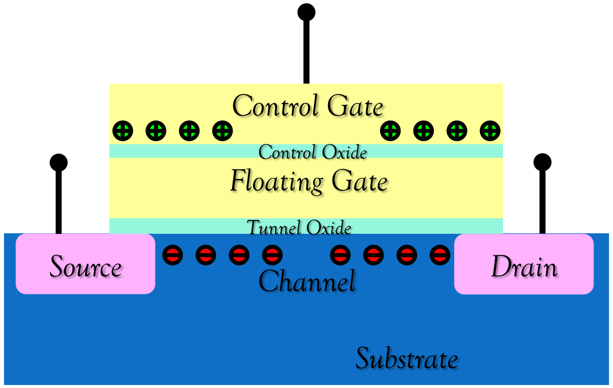
Flash Memories

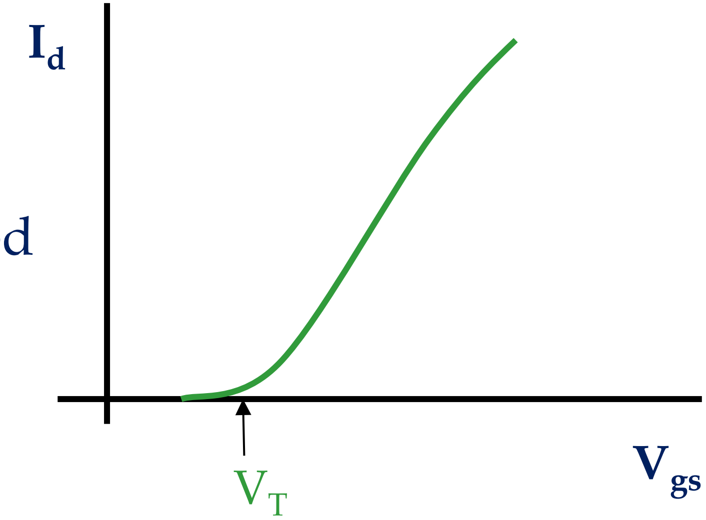


A Flash cell is basically a single floating-gate MOS transistor, i.e., a transistor with a gate completely surrounded by a insulating layer, the floating gate, and electrically governed by a capacitively coupled control gate.

Flash Memories: working principle

Writing process

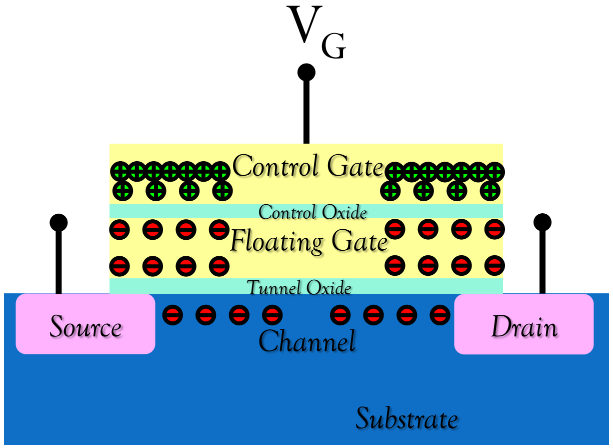




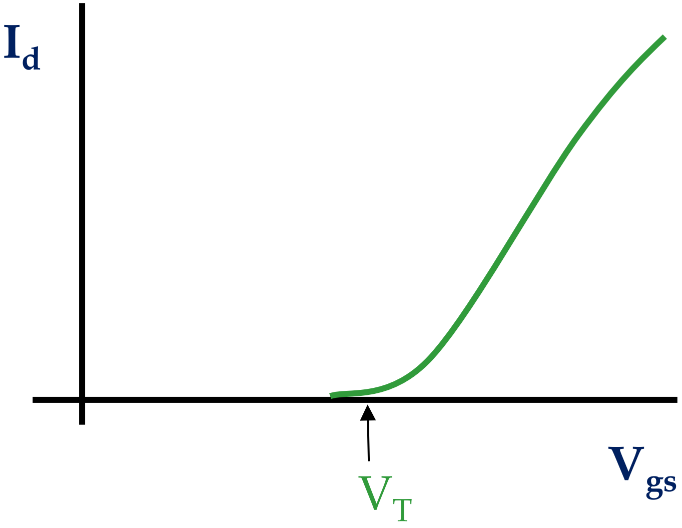
The application of voltage pulses to the *control gate* allows electrons from the *channel* to cross the *tunnel oxide* and charge the *floating gate* (modifying the *threshold voltage* V_t). Thus, the electrostatic potential of the floating gate screens the electrons of the channel, and the current between *source* and *drain* is substantially reduced.

Flash Memories: working principle

Writing process



Programmed



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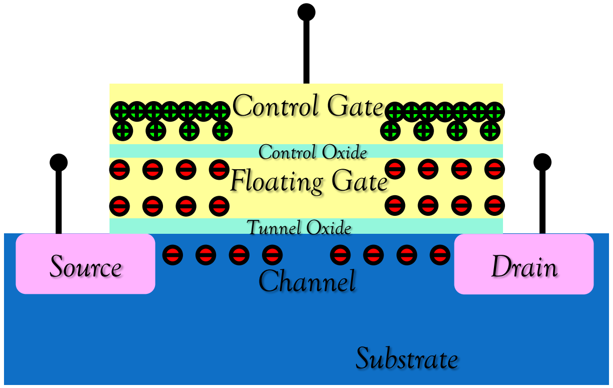
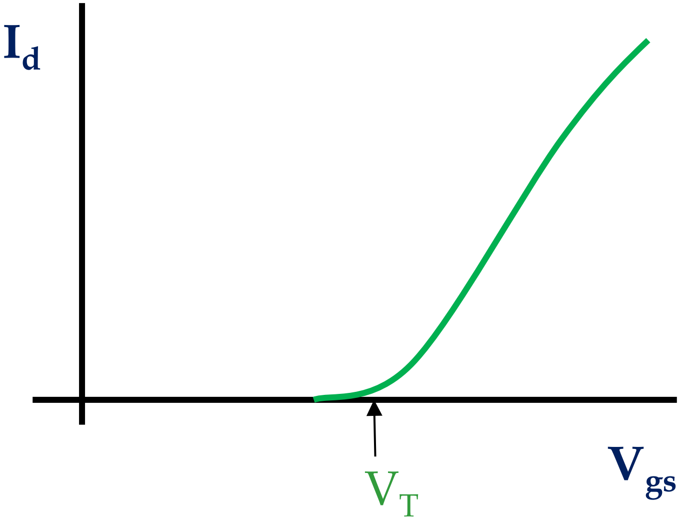
Flash Memories: working principle

Erase process



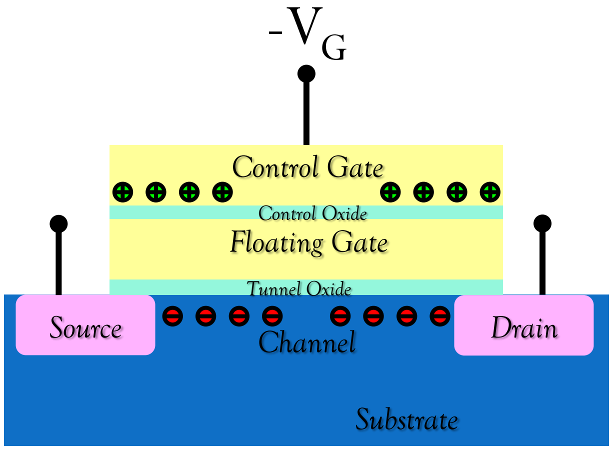
Programmed



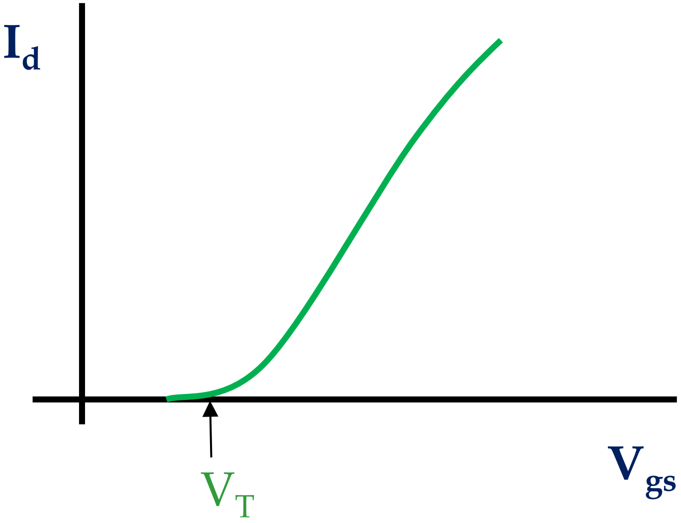
To remove the electrons from the floating gate, an opposite polarity voltage pulse is applied, which brings them back to the channel through the tunnel oxide. In this case, we observe that the source–drain current increases again.

Flash Memories: working principle

Erase process



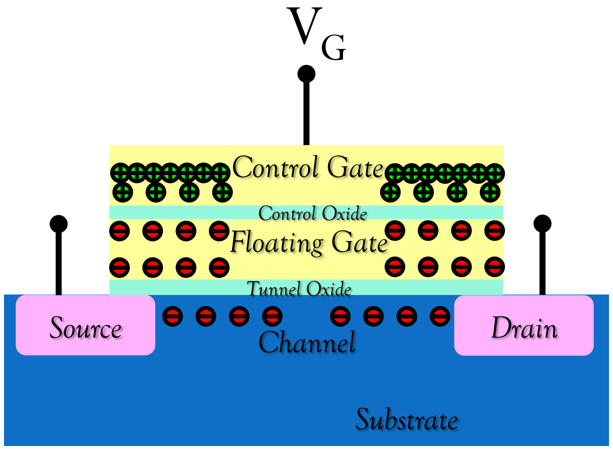
Deleted



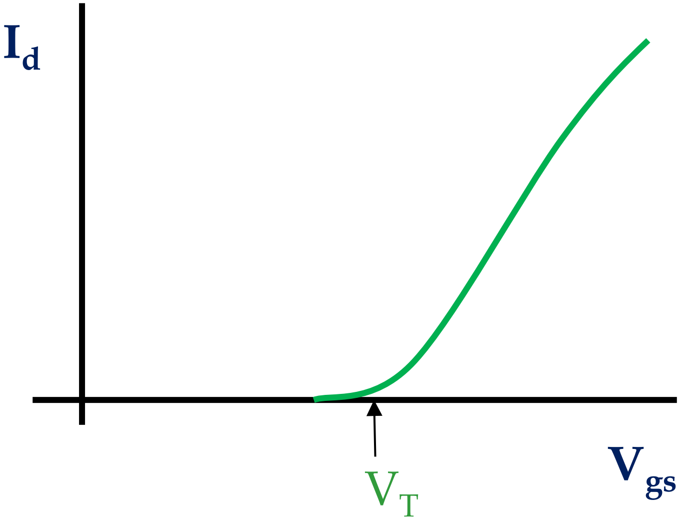
To remove the electrons from the floating gate, an opposite polarity voltage pulse is applied, which brings them back to the channel through the tunnel oxide. In this case, we observe that the source–drain current increases again.

Flash Memories: working principle

Reading process



Programmed



The reading operation is performed evaluating the threshold voltage of the floating gate through the measurement of the drain current at a gate voltage that will not disturb the writing and erasing states of the device.

Conventional memory techonologies

Conventional memory techonologies

Users require

Continuos flow of:

- Faster
- Cheaper
- Smaller

high-technology products

Development of

- High density and fast
- Low cost
- Non-volatile
- Lower power consumption

Memory devices

Conventional memory techonologies

Volatile RAMs

- SRAM
- DRAM

Largest part of the semiconductor memory market

ROMs

- WROM
- UVEPROM
- EEPROM
- FLASH

Some important disadvantages

DRAM

- Volatility
- Power consumption

SRAM

- Volatility
- High cost/bit

FLASH

- Limited program time (ms)
- High cost/bit
- Large programming voltages (> 10 V)

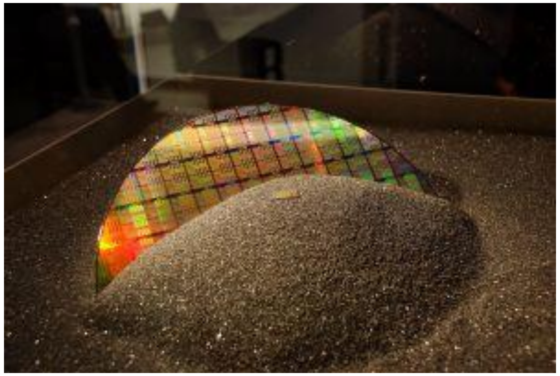
Emerging memory techonologies

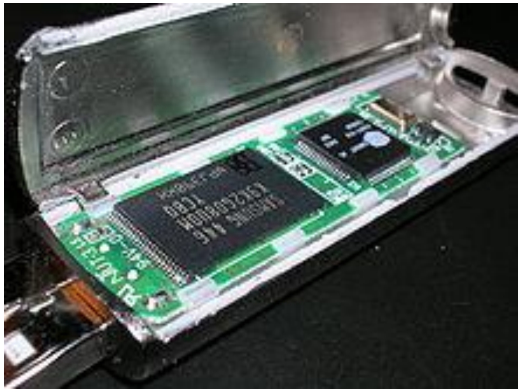
The focus of research is on obtaining *non-volatile*, *fast*, *high-density*, *low-power consumption*, *high data transfer rate* and *reliable* **memory devices**.

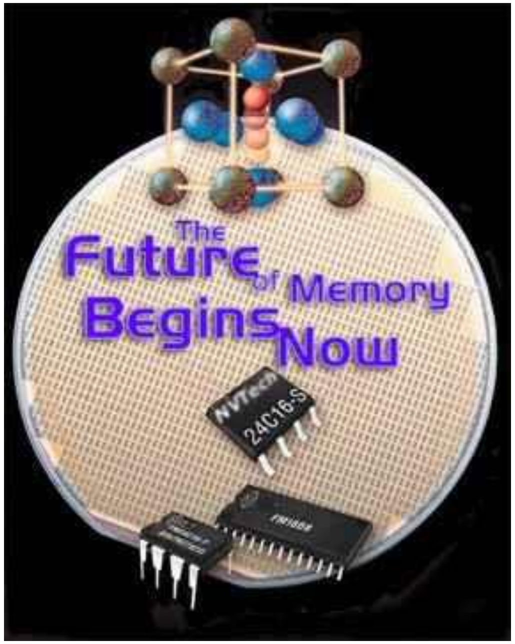
- **FRAM**
- **MRAM**
- **PRAM**
- **RRAM**

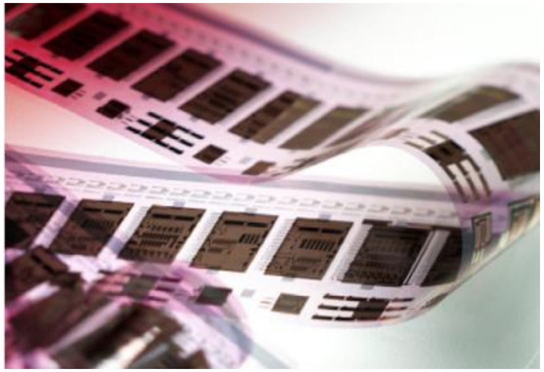
Emerging memory techonologies

The focus of research is on obtaining *non-volatile, fast, high-density, low-power consumption, high data transfer rate* and *reliable* **memory devices**.









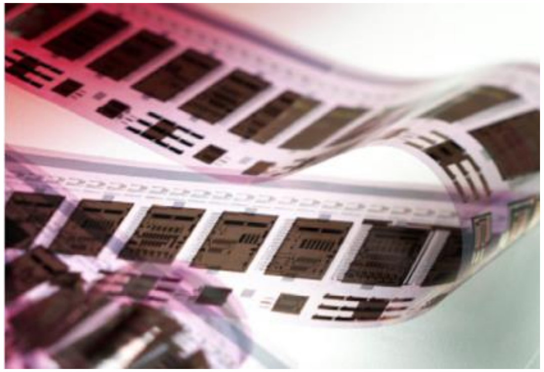
Inorganic electronics Towards **Organic electronics**

Emerging memory techonologies

The focus of research is on obtaining *non-volatile*, *fast*, *high-density*, *low-power consumption*, *high data transfer rate* and *reliable* **memory devices**.

Why Organic Electronics?

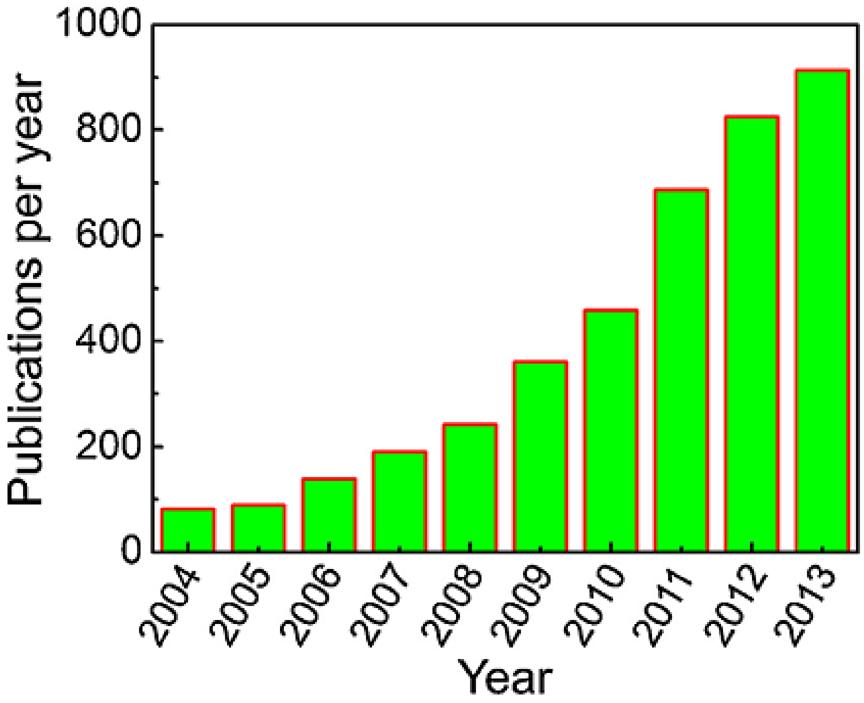
- simple fabrication
- low cost manufacturability
- mechanical flexibility and stretchability
- low-temperature fabrication process
- printability for mass industrial production

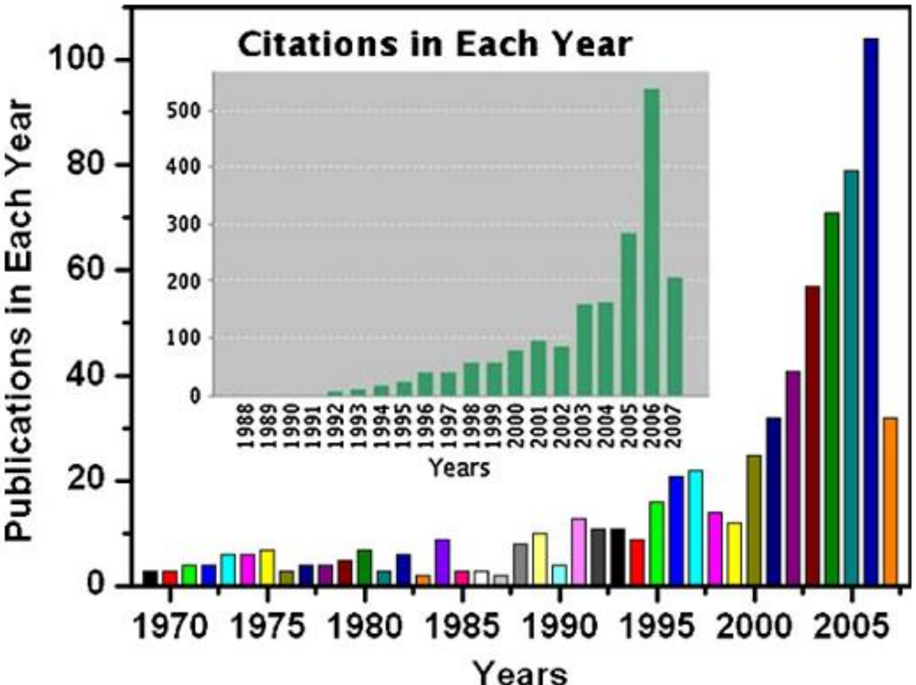


Organic electronics

Potential and challenges of organic memory devices

- ✓ Polymer electronic memories were first reported in 1970: from then, a wide variety of polymers have been reported to show memory behavior
- ✓ Many of the earlier memory effects showed unsatisfactory performance for practical application
- ✓ A rapid growth in the interest in organic memories in the last 15 years

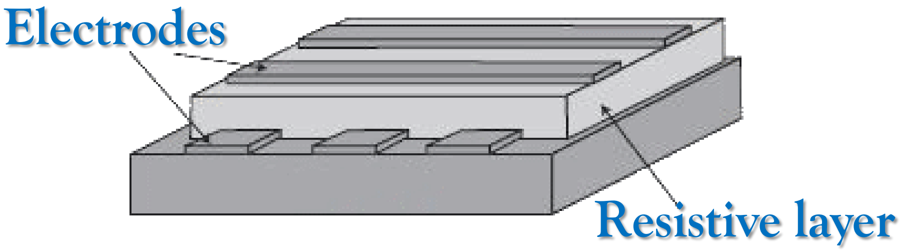




Organic memory structures

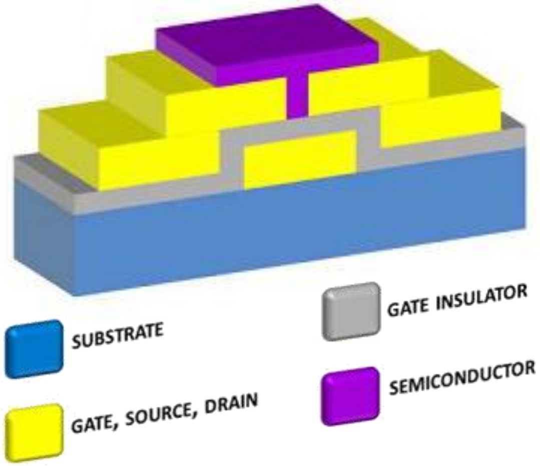
Organic memory devices that have so far appeared in the literature:

- **two-terminal bi-stable devices (resistive memories)**



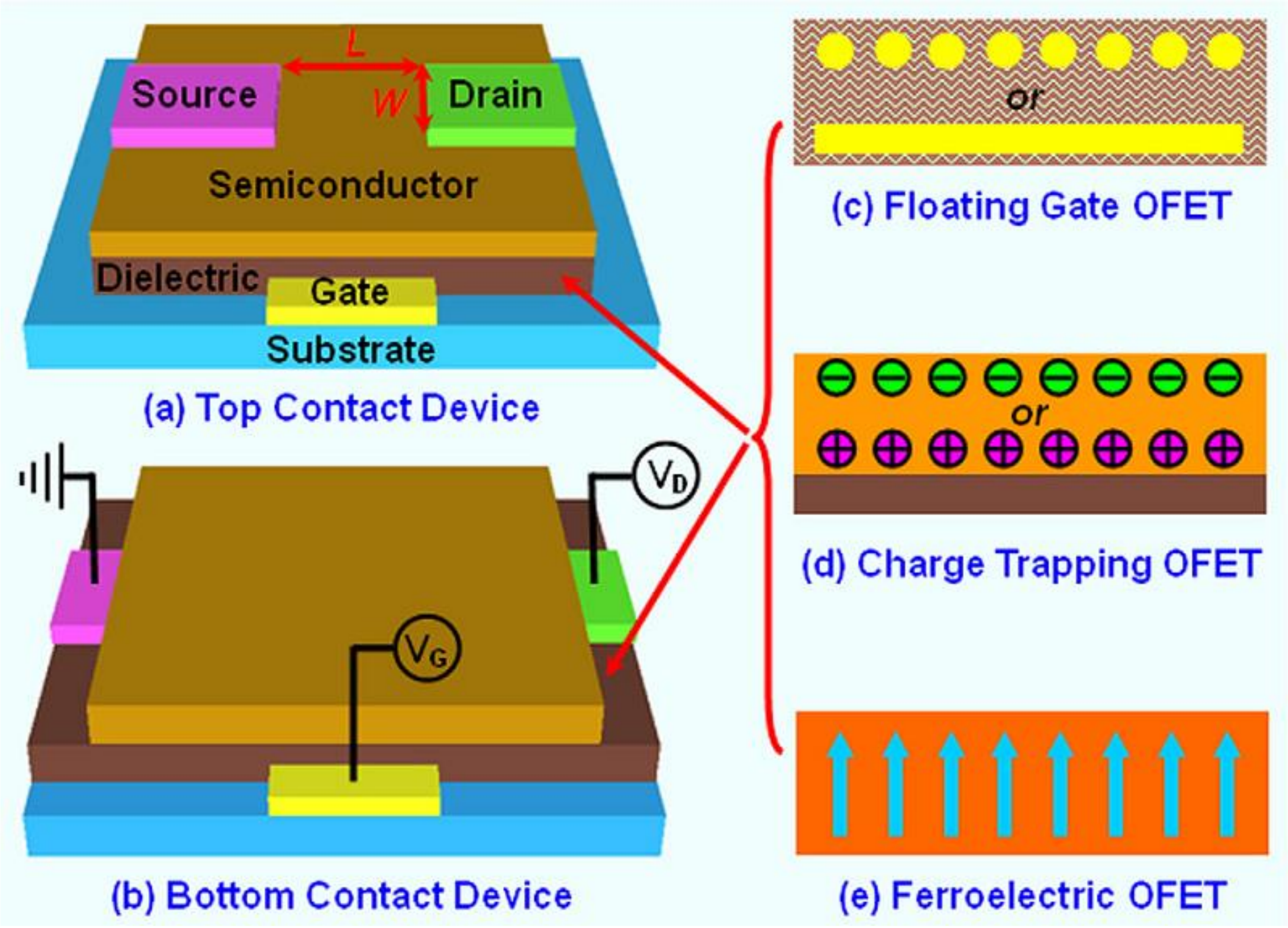
Resistance can be (reversibly) switched between low and high states (*resistive switching*) by appropriate voltage pulses

- **three-terminal devices (transistor memories)**



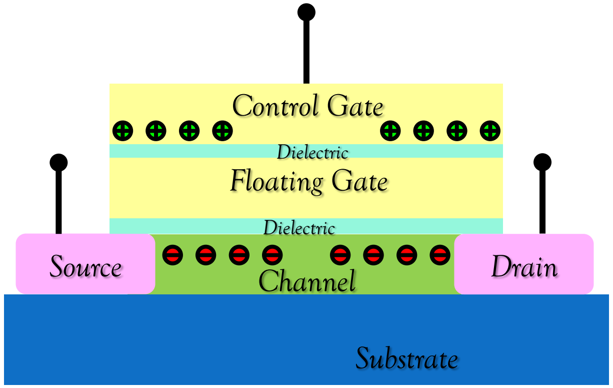
Memory effect is obtained by inducing charge storage in different areas of the device, thus resulting in a shift of the threshold voltage or hysteresis in the transfer curve.

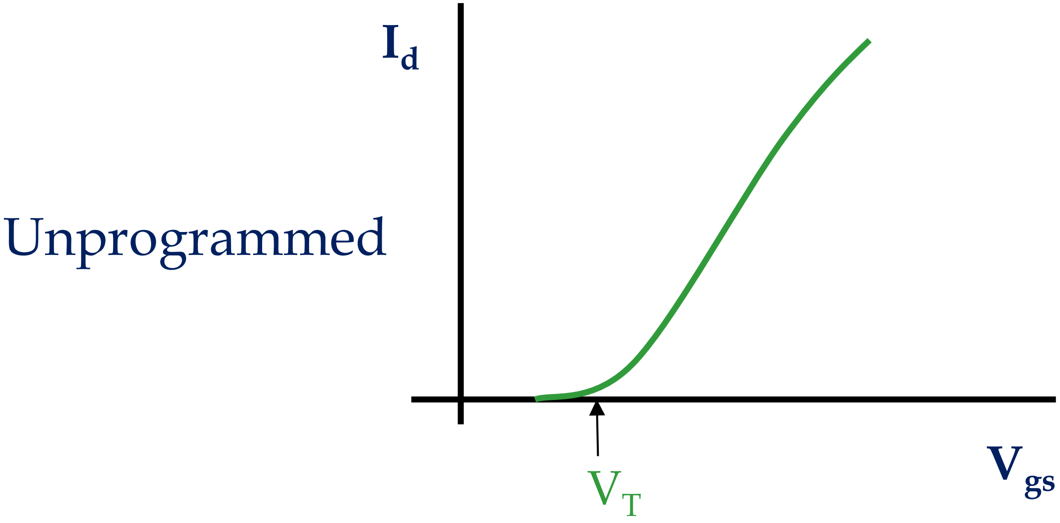
Organic Transistor-type memories



Floating gate OFET memories

Working principle

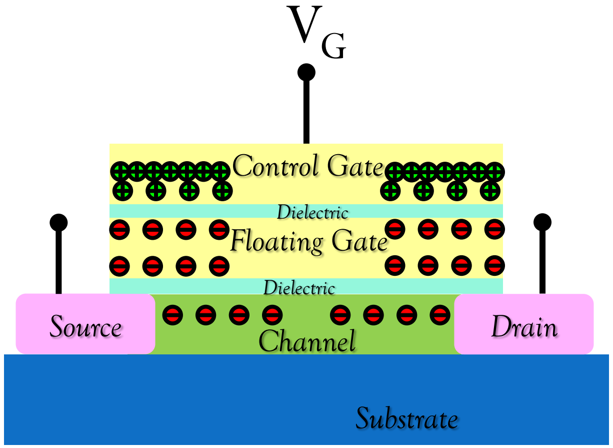




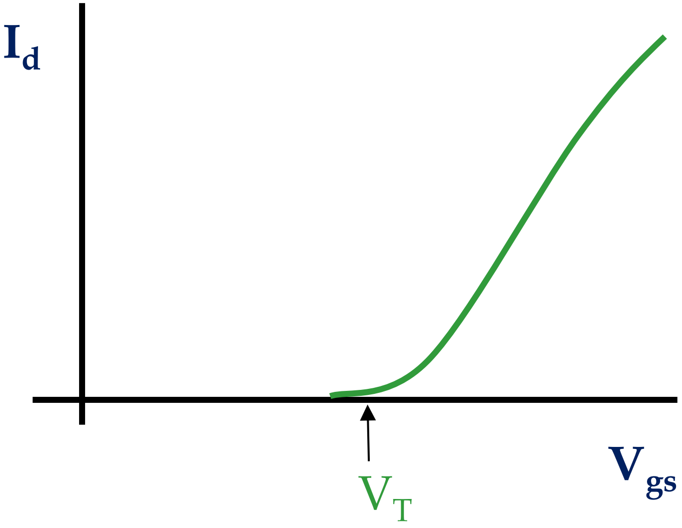
- The **dielectric layer between the floating gate and the semiconductor** must be **very thin** in order to allow injection of charges toward the floating gate
- The **dielectric layer between the floating gate and the gate** electrode must be **thick enough** to prevent discharge when V_G is removed.

Floating gate OFET memories

Working principle



Programmed

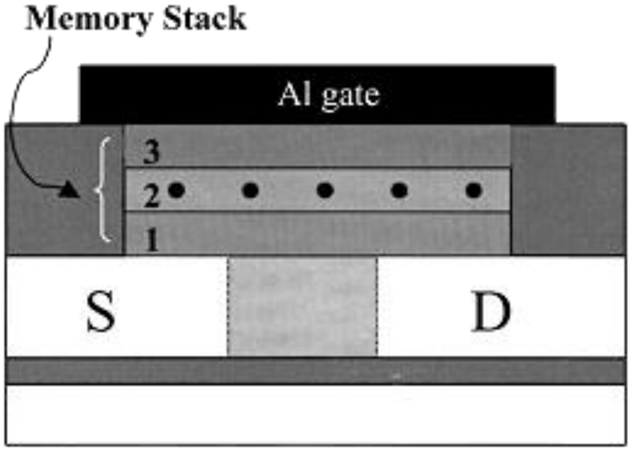


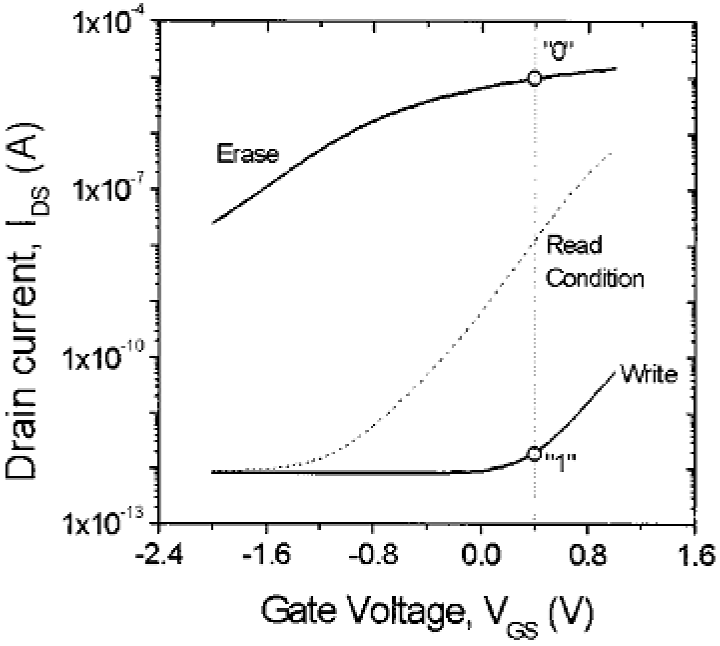
- The **dielectric layer between the floating gate and the semiconductor** must be **very thin** in order to allow injection of charges toward the floating gate
- The **dielectric layer between the floating gate and the gate** electrode must be **thick enough** to prevent discharge when V_G is removed.

Floating gate OFET memories

2003

- Hybrid silicon–organic memory device using gold nanoparticles as charge storage elements
- Nanoparticles are separated from the silicon channel by a SiO_2 layer and from the gate electrode by an **organic insulator**



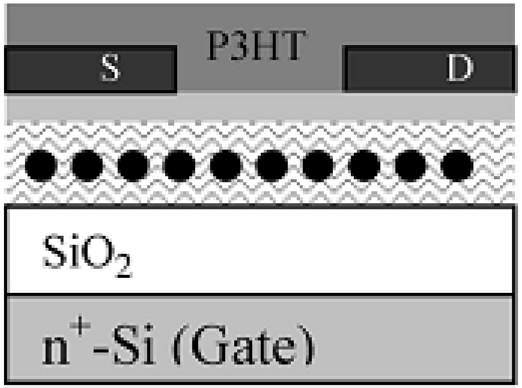


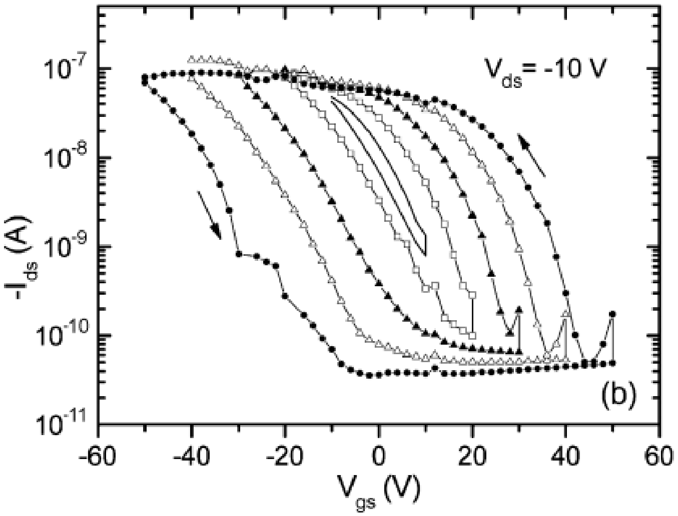
Kolliopoulou et al., Journal of Applied Physics, 94(8):5234–5239, 2003.

Floating gate OFET memories

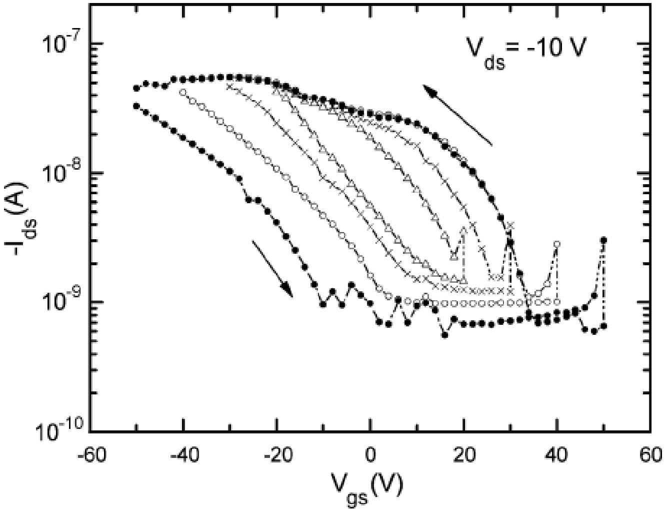
2006

- Integration of a gold nanoparticles film into the gate dielectric of an OFET to produce memory effects
- Gold nanoparticles behave as the floating gate for charge storage
- Charge storage in the Au NPs is confirmed by comparing the electrical characteristics with those of the Au NP-free
- Retention time: 200 seconds





Device with Au NPs



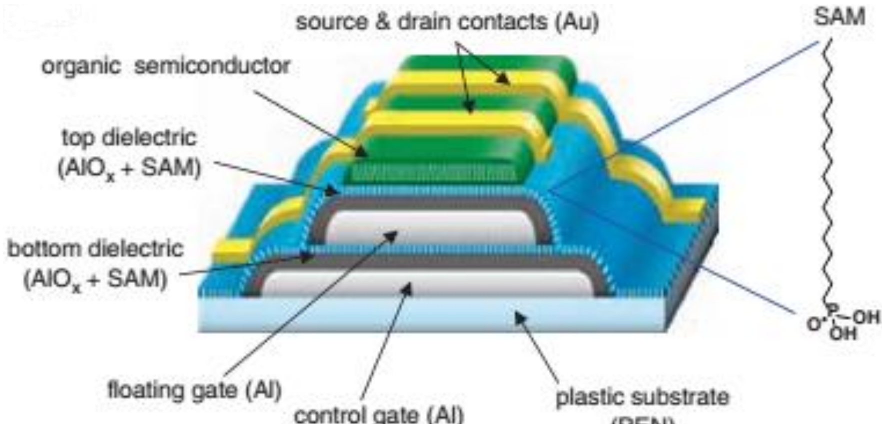
Device without Au NPs

Liu et al., Nanotechnology, IEEE Transactions on, 5(4):379–384, July 2006

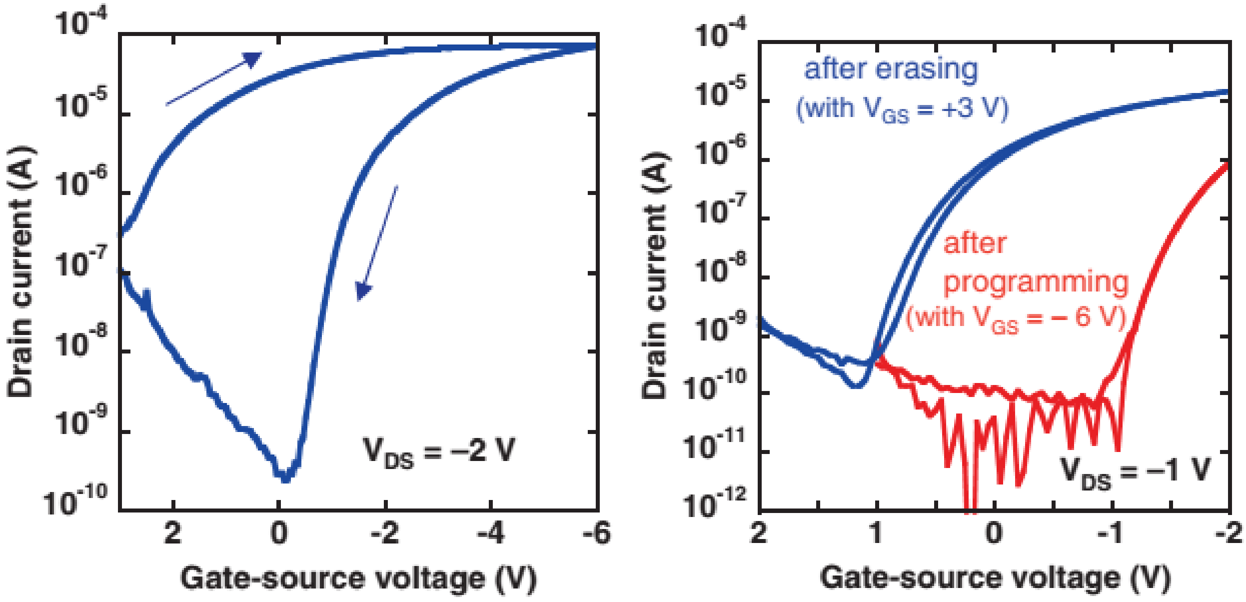
Floating gate OFET memories

2009

- Flexible floating gate transistors with small programming voltages (-6 V to +3 V)
- Control and floating gate made of aluminum



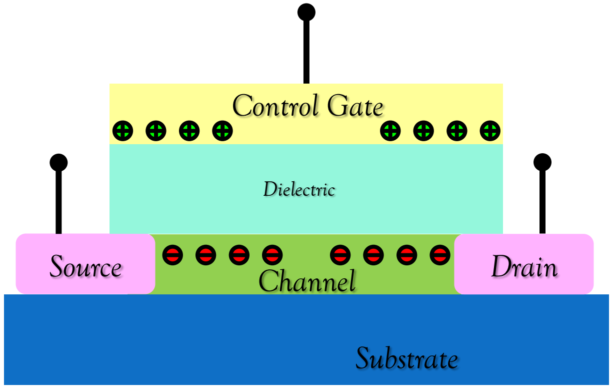
- Dielectric made of an aluminum oxide layer and a SAM
- One of the **best result** reported to date for floating gate OFET memories
- Retention time: 12 hours

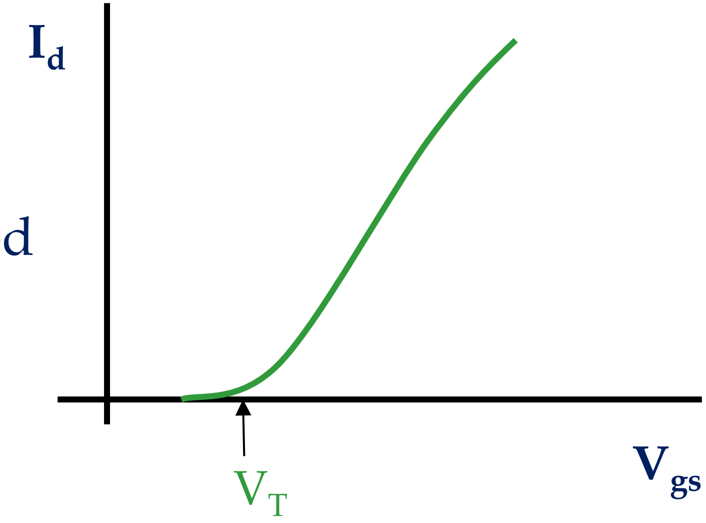


Sekitani et al., Science, 326(5959):1516–1519, 2009

Charge-trapping OFET memories

Working principle

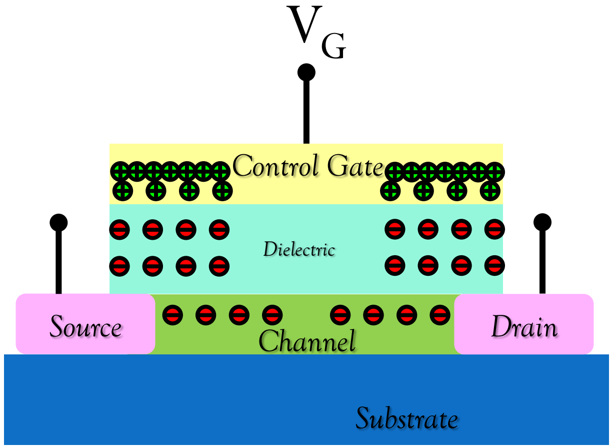




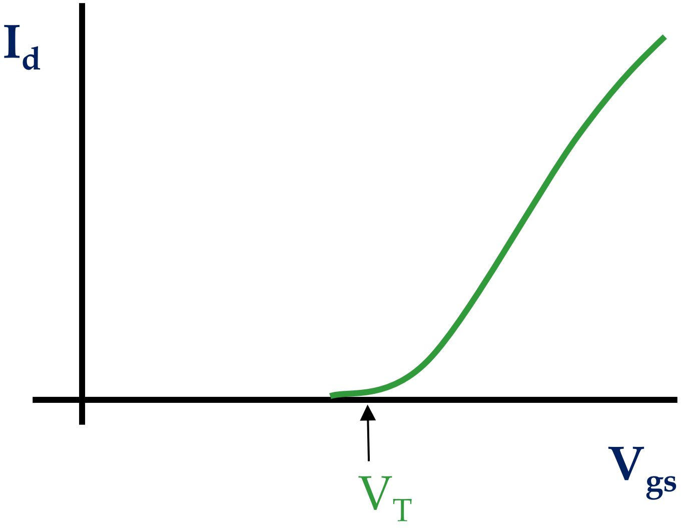
- **Charge carrier** is **stored** in an appropriate **dielectric layer (electret)** which has a quasi – permanent electric charge or dipolar polarization

Charge-trapping OFET memories

Working principle



Programmed

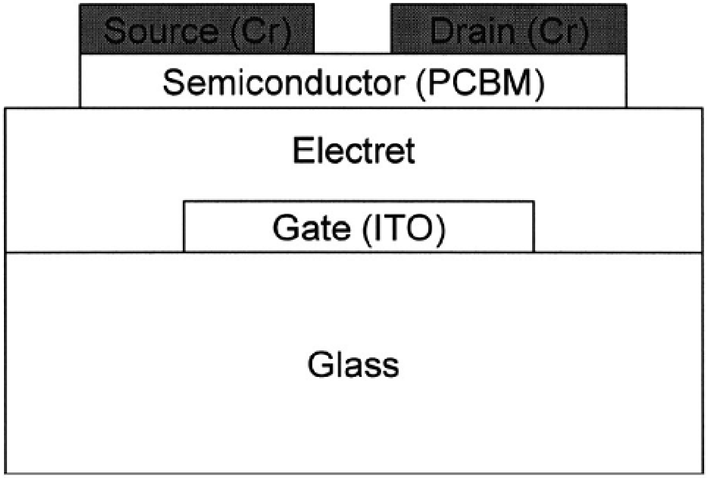


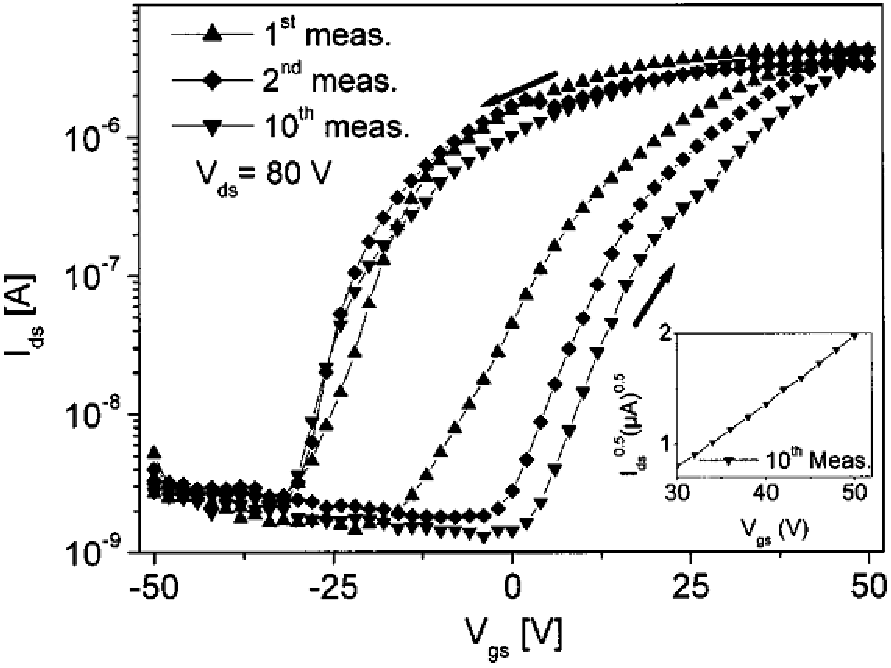
- **Charge carrier** is **stored** in an appropriate **dielectric layer (electret)** which has a quasi – permanent electric charge or dipolar polarization

Charge trapping OFET memories

2004

- First OFET memory containing an electret as gate insulator (Polyvinyl alcohol or PVA)
- Large hysteresis in the transfer characteristics cycling the gate voltage
- Retention time: 15 hours



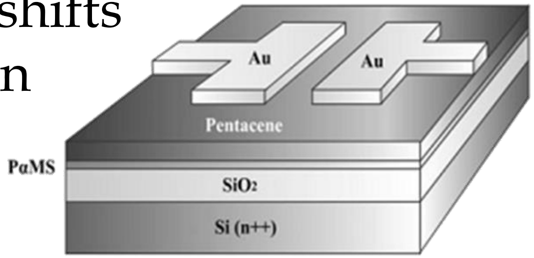


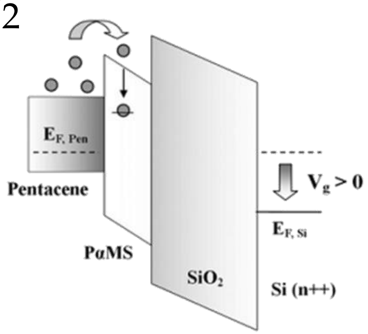
Singh et al., Applied physics letters, 85(22):5409–5411, 2004.

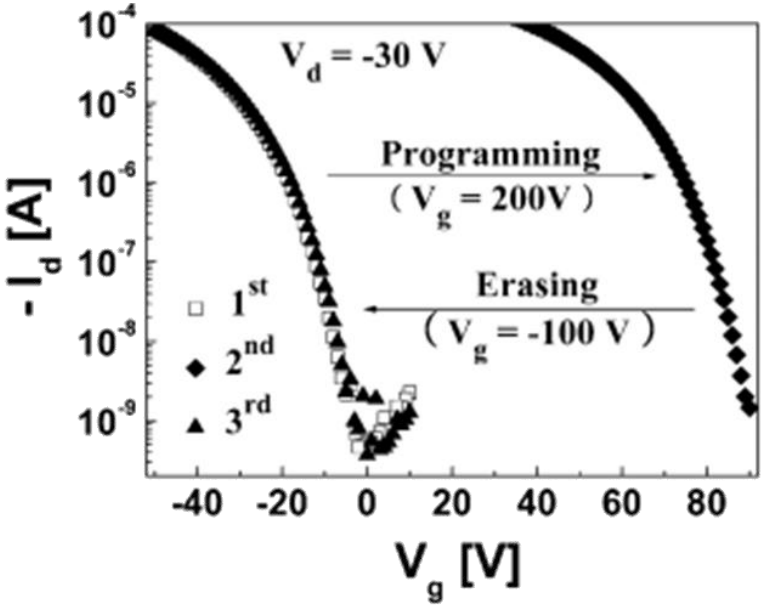
Charge trapping OFET memories

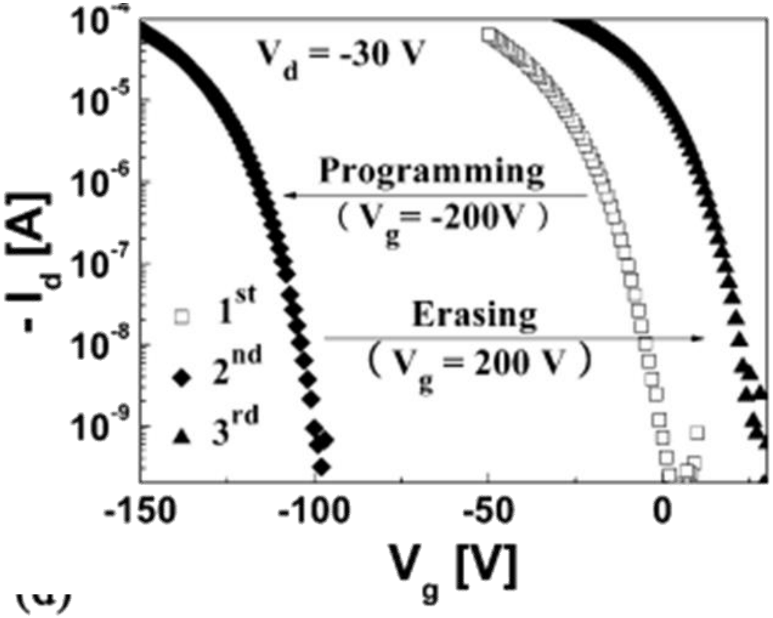
2006

- **By-layer dielectric**: hydrophobic polymer PαMS and SiO_2
- Positive and negative direction shifts
- Shifts can be obtained only when PαMS is inserted between SiO_2 gate insulator and the channel
- Retention time: 100 hours







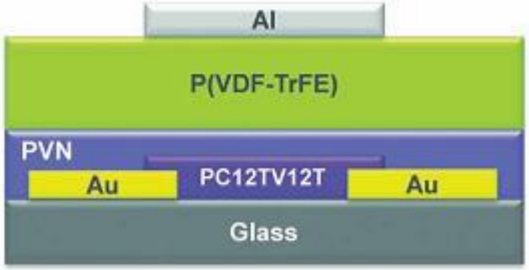


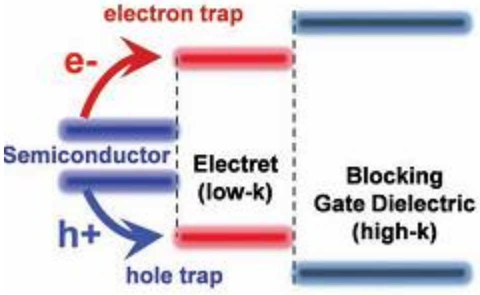
Baeg et al., Advanced Materials, 18(23):3179–3183, 2006.

Charge trapping OFET memories

2012

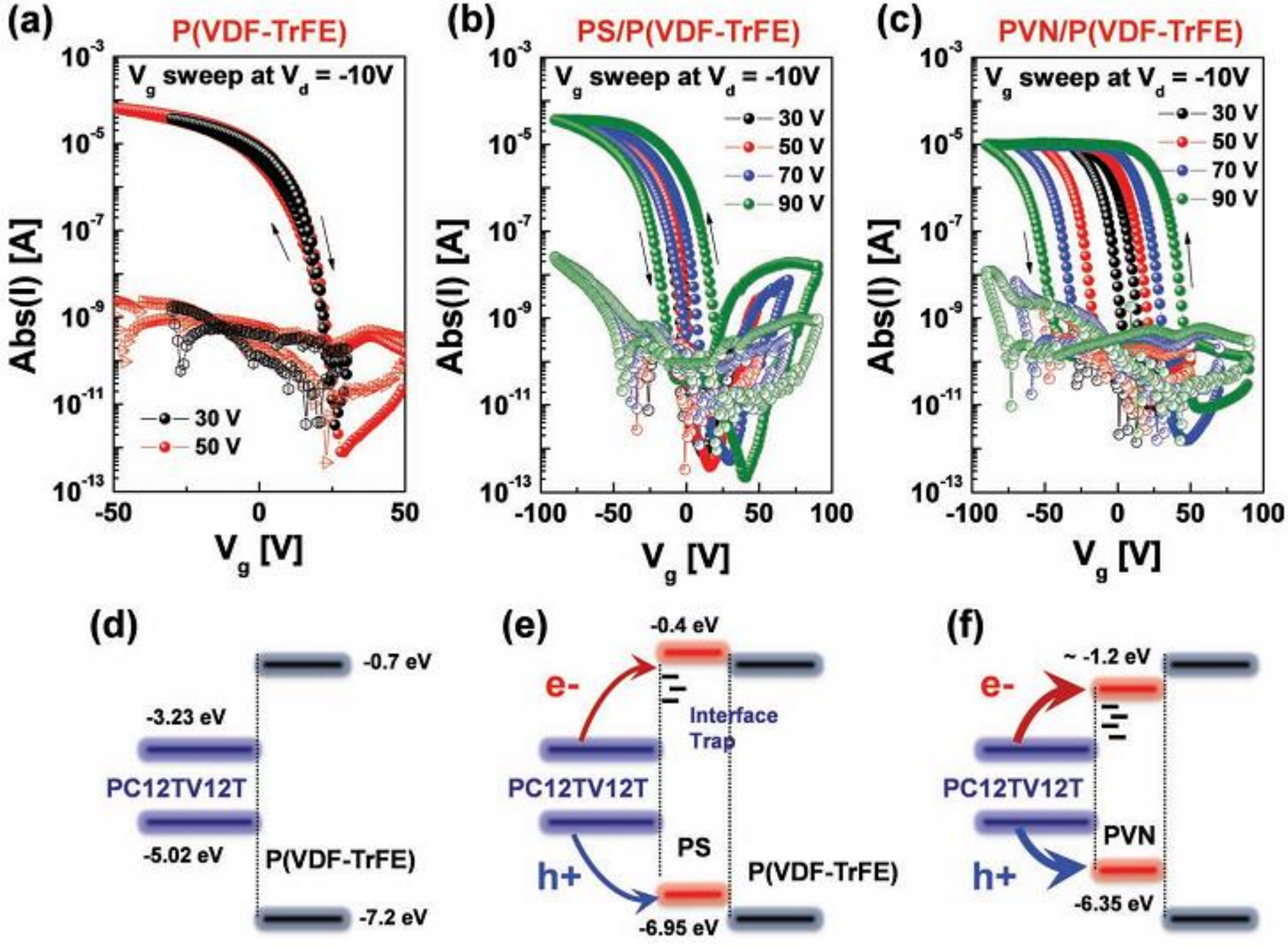
- High-performance top-gated OFET memory with **bylayered polymer dielectrics** (P(VDF-TrFE) and PVN or PS)
- Excellent non-volatile memory characteristics with P(VDF-TrFE)/PVN dielectric: high ON/OFF current ratio(∽ 10^5), a relatively low operation voltage of less than 20 V, and a long retention time of ∽ 10^7 s (less then 4 months)
- Efficient and reversible charge trapping and release in the PVN layer
- Memory characteristics effectively disappeared replacing PVN with PS
- Different memory characteristics between devices were attributed to a **different alignment of the energy levels** for the charge transfer from the semiconductor to the PVN or PS layer





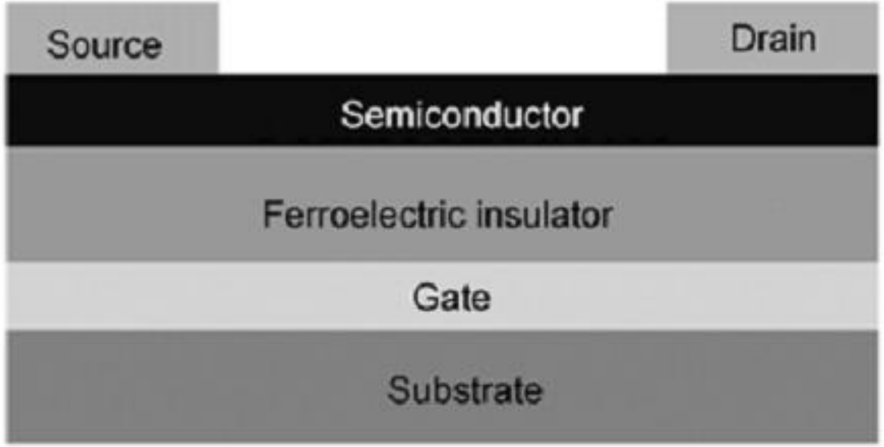
Baeg et al., Advanced Functional Materials, 22(14):2915–2926, 2012.

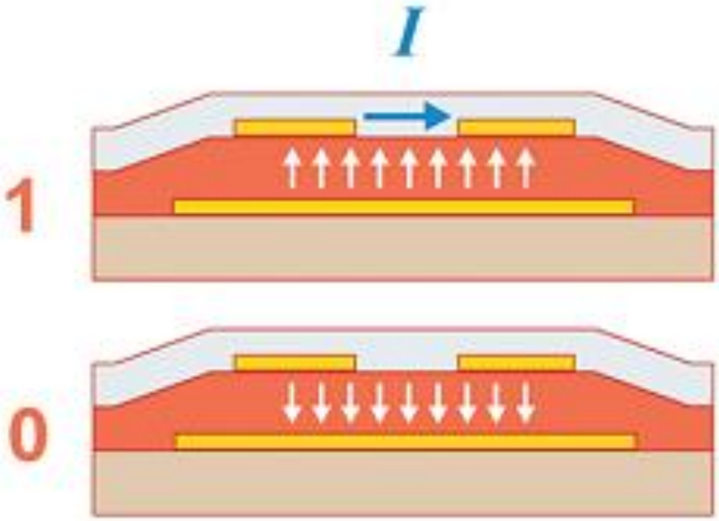
Charge trapping OFET memories



Ferroelectric OFET memories

- Ferroelectric material as gate dielectric
- Two stable polarization states: switching from one polarization state to the other can occur by applying a sufficiently large gate bias
- Depending on the direction of the polarization, positive or negative counter charges are induced at the semiconductor-ferroelectric interface, causing a positive or negative onset voltage shift of the transistor





Ferroelectric OFET memories

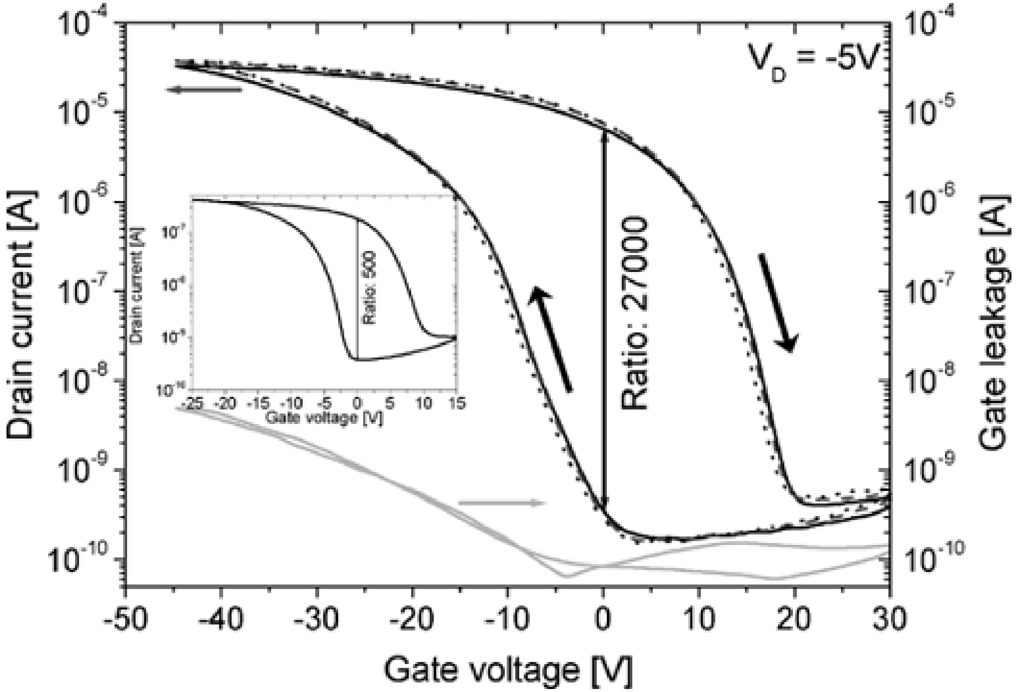
1986

- First FET based on a polymeric ferroelectric

2004-2005

- All organic FET devices incorporating a ferroelectric-like polymer as the gate insulator and pentacene as the organic semiconductor were first reported
- A clear hysteresis in transfer characteristic
- Retention time: few days

Schroeder et al., Electron Device Letters, IEEE, 26(2):69–71, Feb 2005.

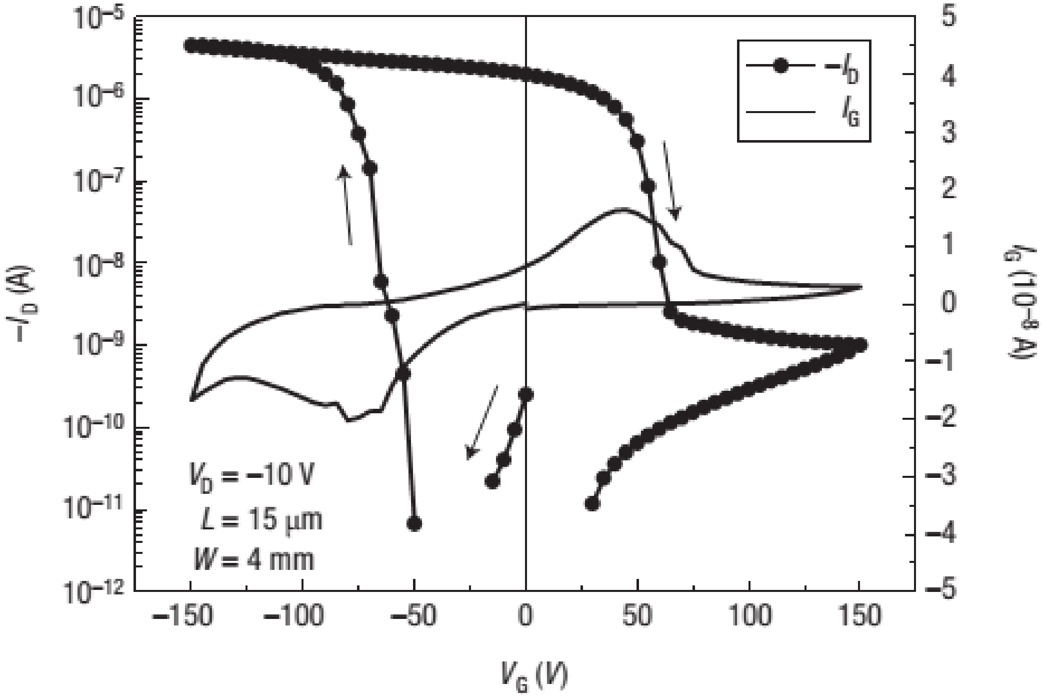


Ferroelectric OFET memories

2005

- High-performance solution-processed polymer FeFET memories consisting of P(VDF–TrFE) as the gate insulator
- Operation voltages: ± 60 V and ± 35 V (ferroelectric layer thickness of 1.7 and 0.85 μm)
- Retention time: 1 week

The application of a negative gate bias results in a sharp increase by several orders of magnitude of the channel current associated with hole accumulation and a remanent on-state current after bringing the bias back to zero.



Naber et al., Nature Materials, 4(3):243–248, 2005.

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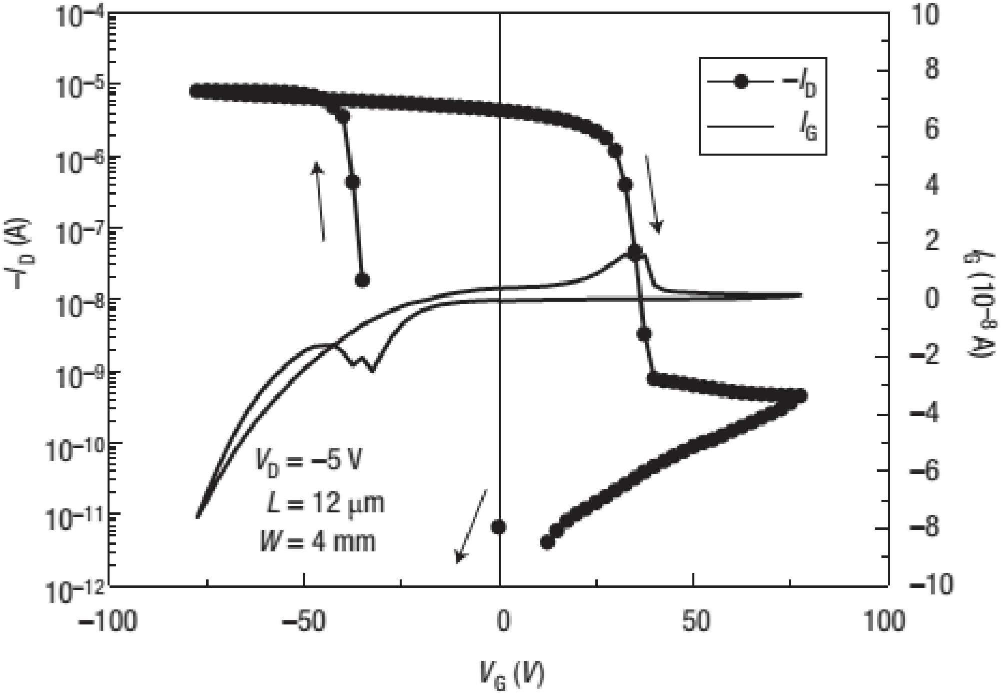
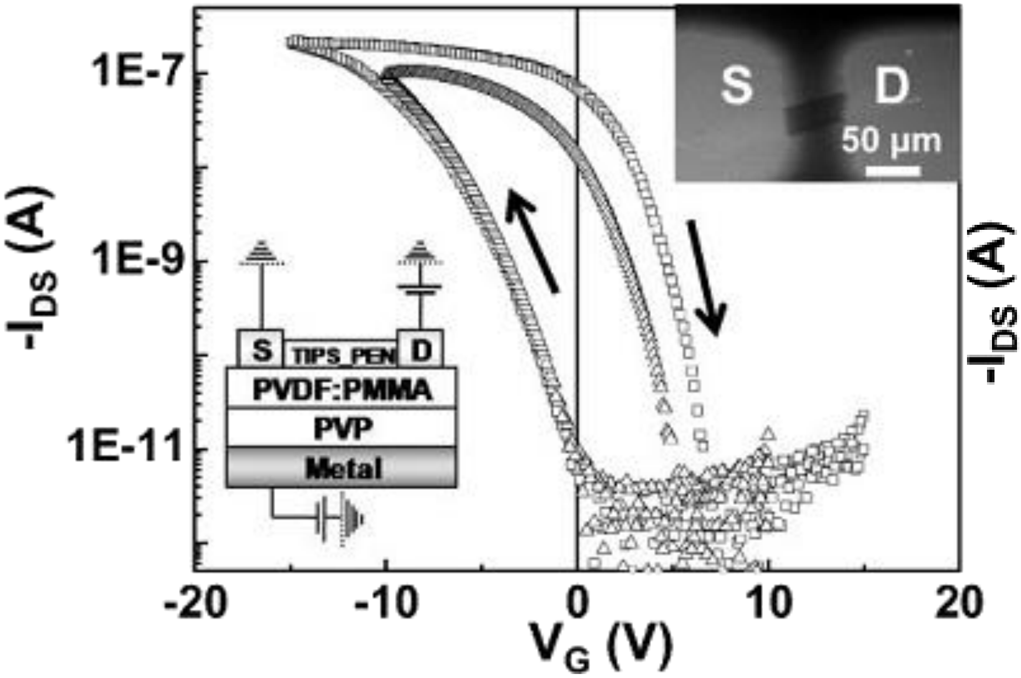


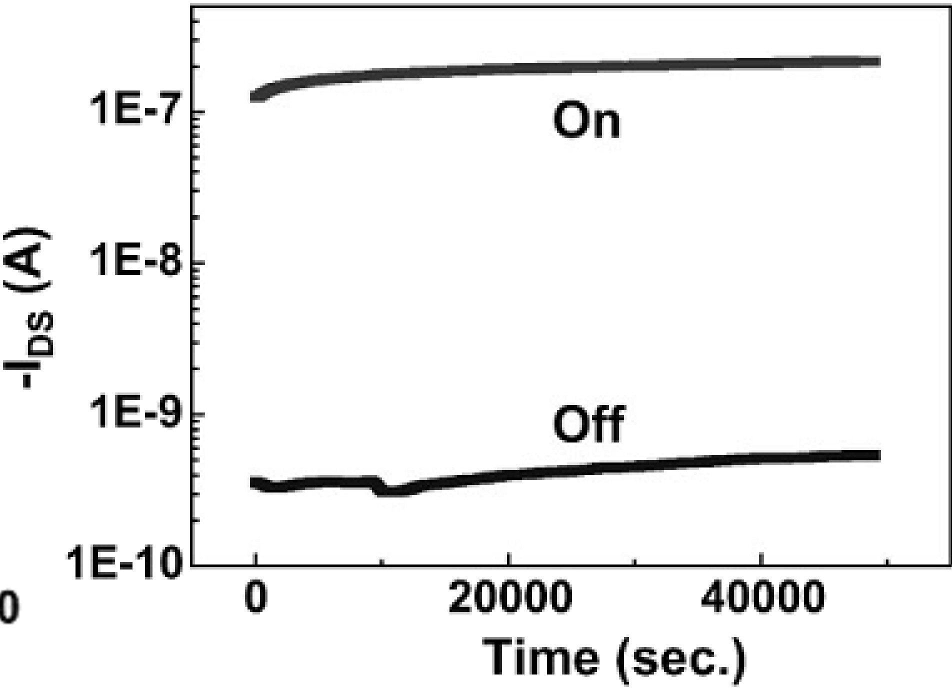
Naber et al., Nature Materials, 4(3):243–248, 2005.

Ferroelectric OFET memories

2009

- Bottom gate FeFET containing PVDF/PMMA blend films of 200 nm
- Operation voltages: 15 V
- Retention time: 15 h





Kang et al., Advanced Functional Materials, 19(17):2812–2818, 2009.

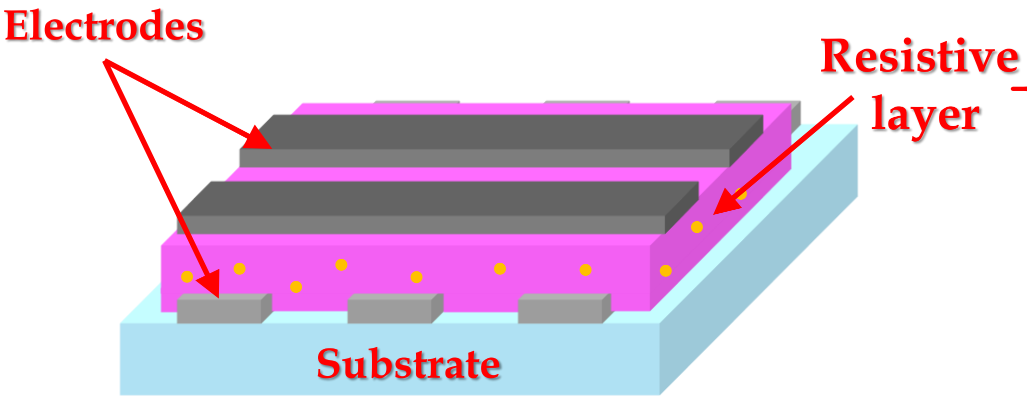
Organic transistor-memories: developmental status

- Tremendous progress has been made in the field of OFET memories since it was first described.
- OFET memories have great potential for application in low cost, large areas, plastic systems, but many challenges are still open:
  - program/read/erase voltages are still large;
  - data retention times are too short to satisfy the requirements of practical applications;
  - operating mechanisms of OFET memories are not clearly understood.
- All of these issues need to be addressed in the future to aid the design of high performance devices.

Organic Resistor-type memories

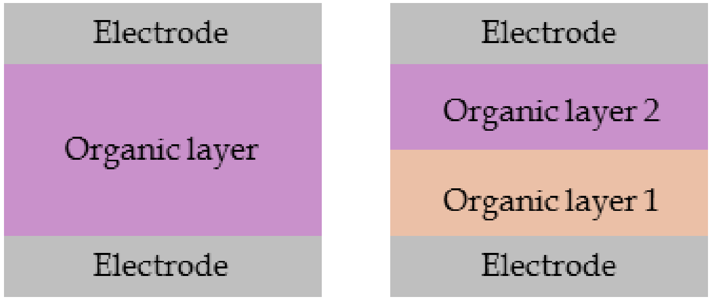
The most promising class of organic two-terminal memories is the **resistive random access memory** (**RRAM**), whose resistance can be (reversibly) switched between low and high states by appropriate voltage pulses

General structure

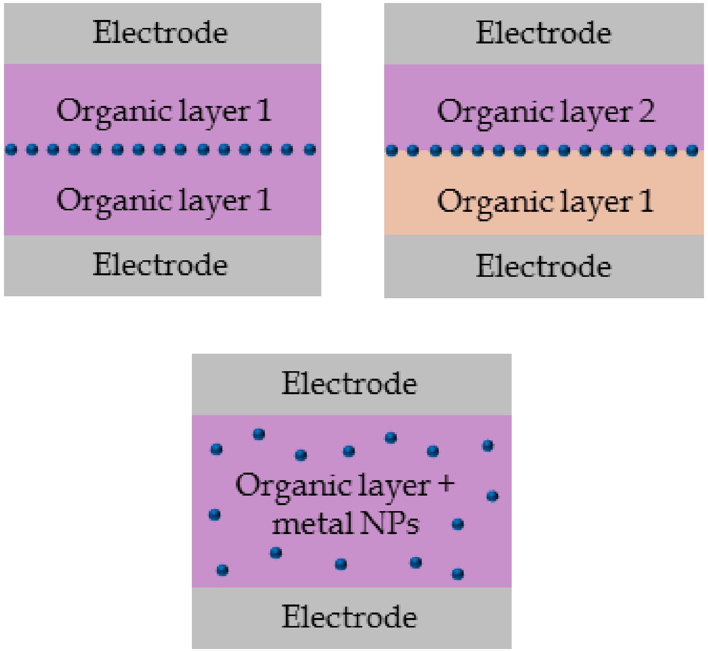


Two terminal elements, consisting of a cross-point array of top and bottom electrodes, separated by a resistive material. Each area where the top and the bottom electrodes cross is a memory cell

Without metal nanoparticles (NPs)

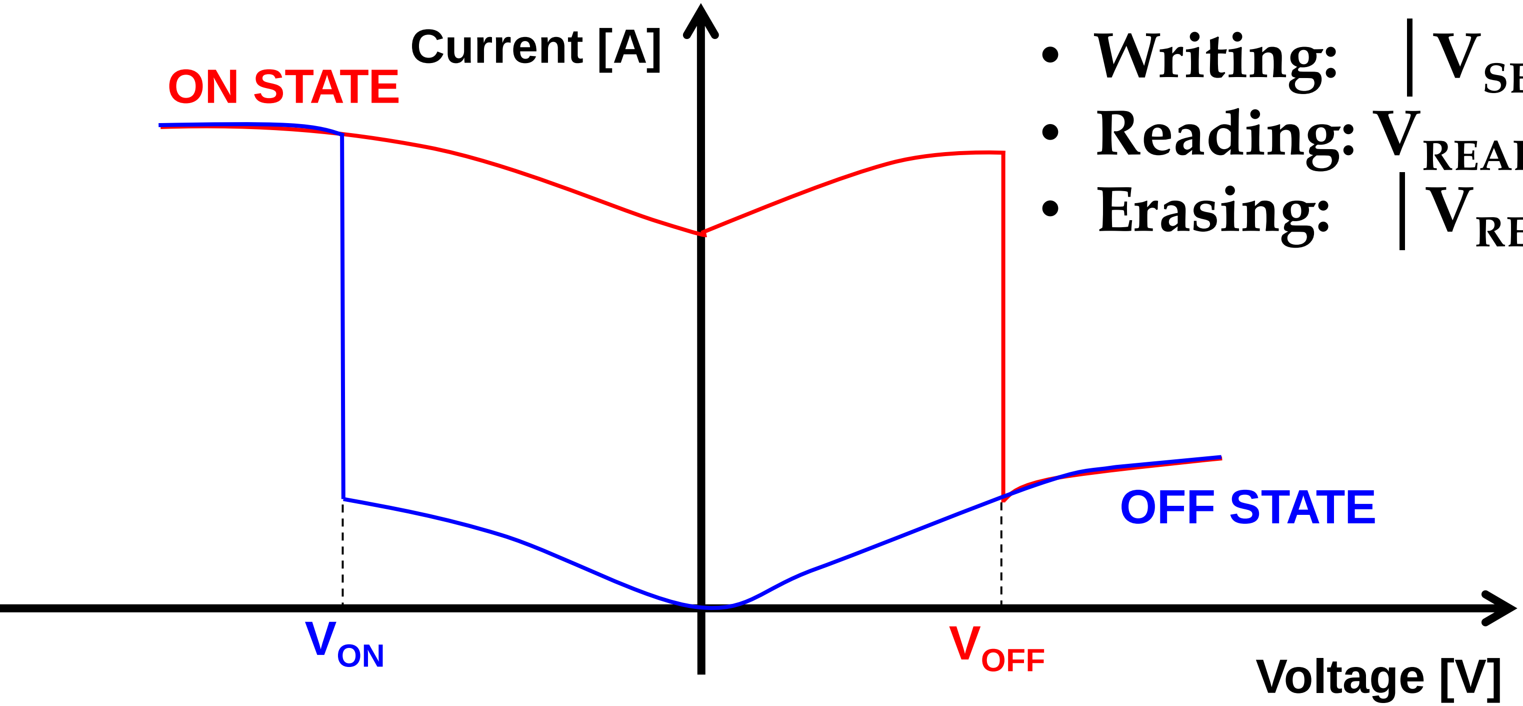


With metal nanoparticles (NPs)



Organic RRAM working principle

Resistive switching

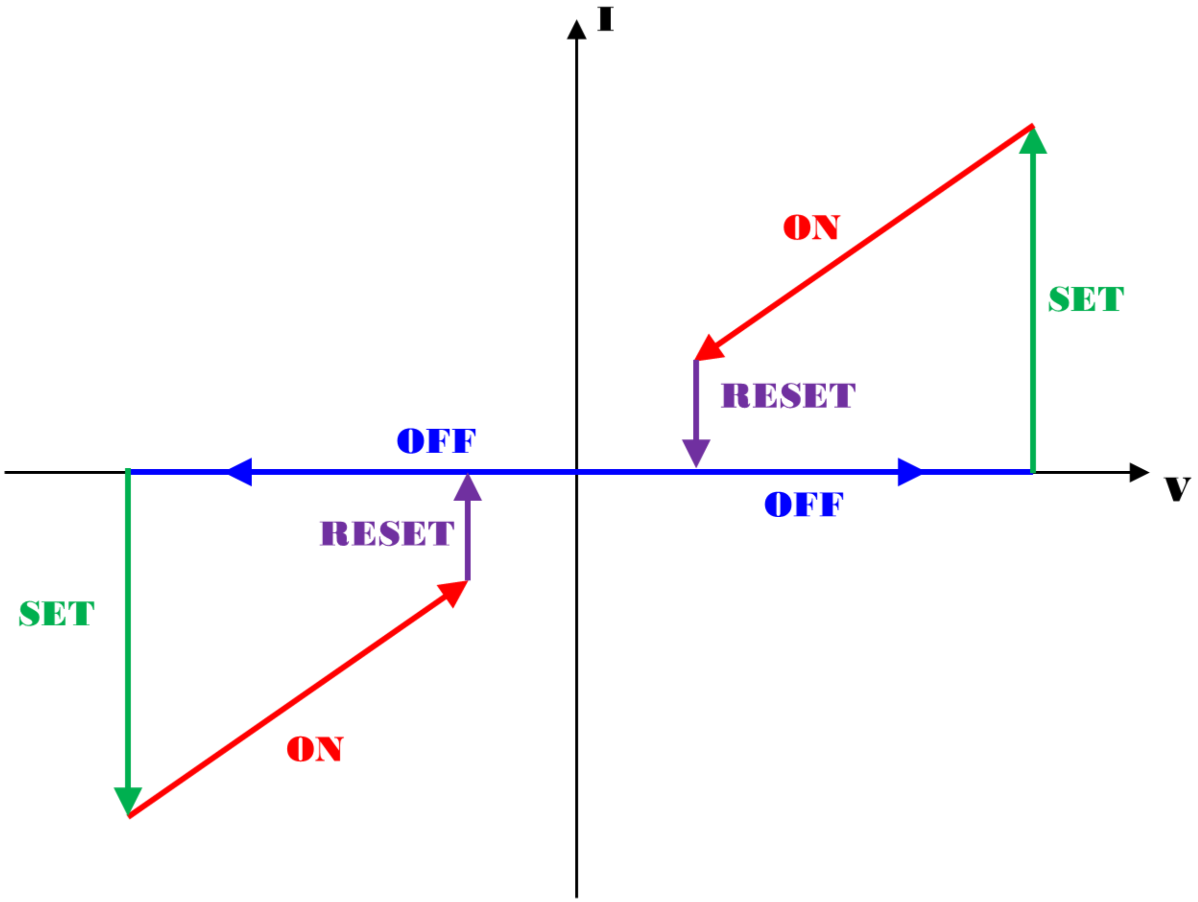


- **Writing:** $|V_{SET}| \geq |V_{ON}|$
- **Reading:** $V_{READ} \sim 0$
- **Erasing:** $|V_{RESET}| \geq |V_{OFF}|$

By applying an appropriate voltage, the resistance of the memory can be reversibly switched between a high resistance state (HRS, or OFF state) and a low-resistance state (LRS, or ON state).

Organic RRAM: electrical characteristics

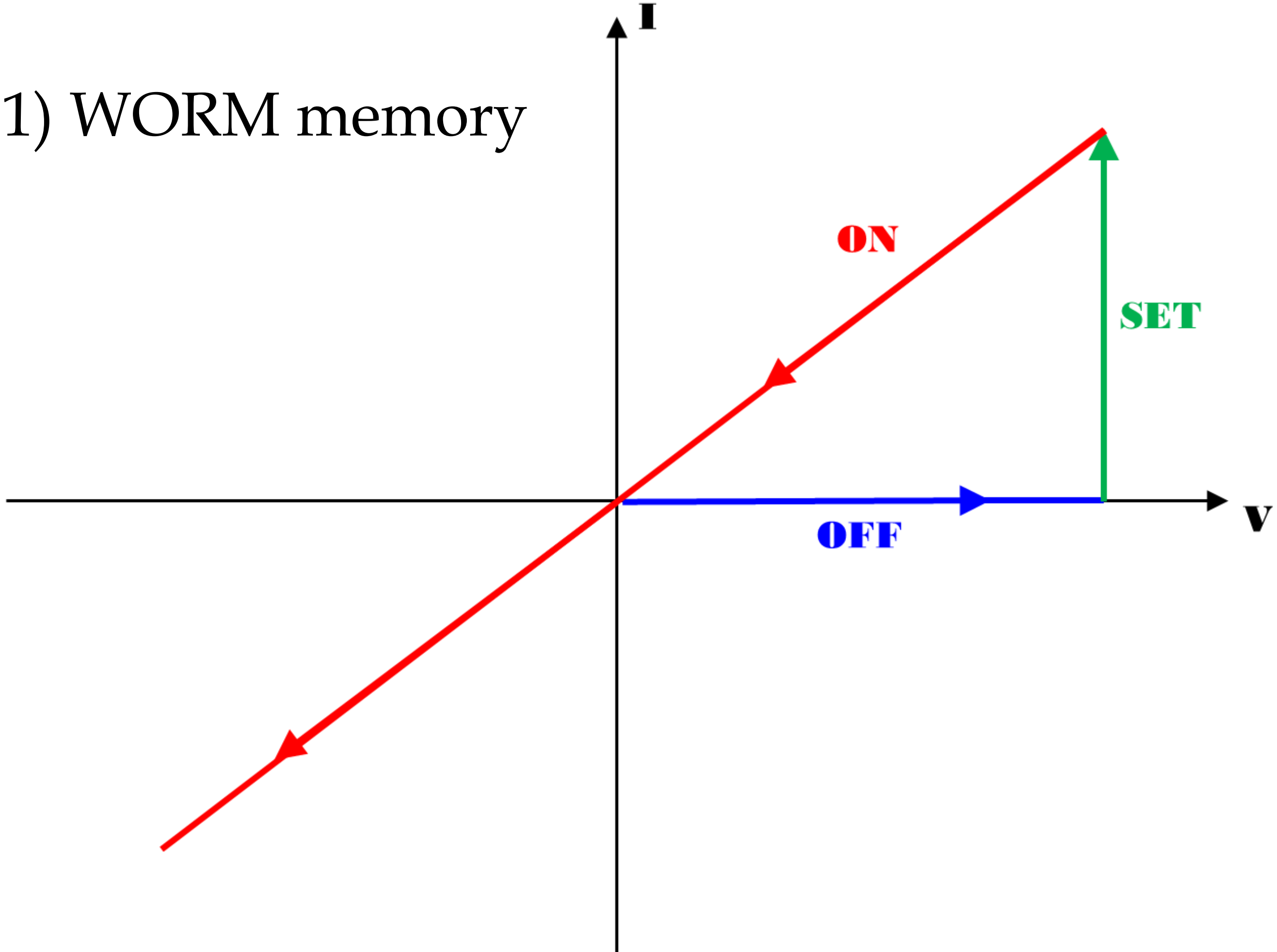
Typical I-V curve of a **volatile** RRAM



Organic RRAM: electrical characteristics

Typical I-V curves of **non-volatile** RRAMs

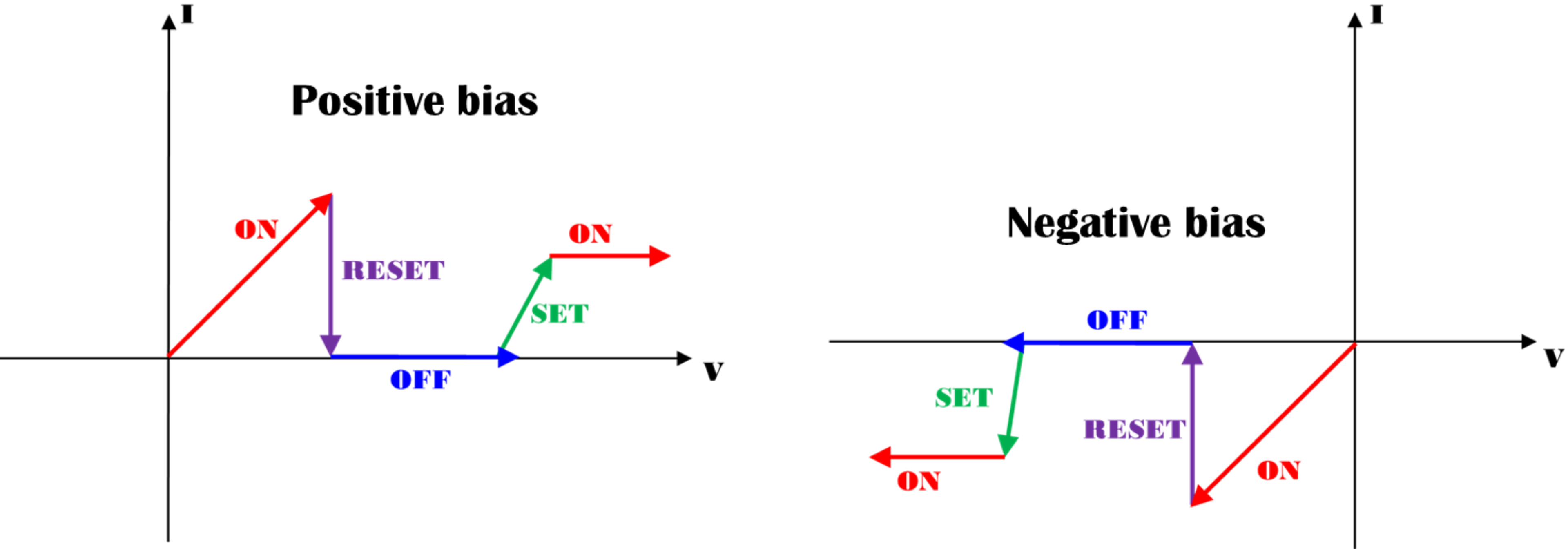
1) WORM memory



Organic RRAM: electrical characteristics

Typical I-V curves of **non-volatile** RRAMs

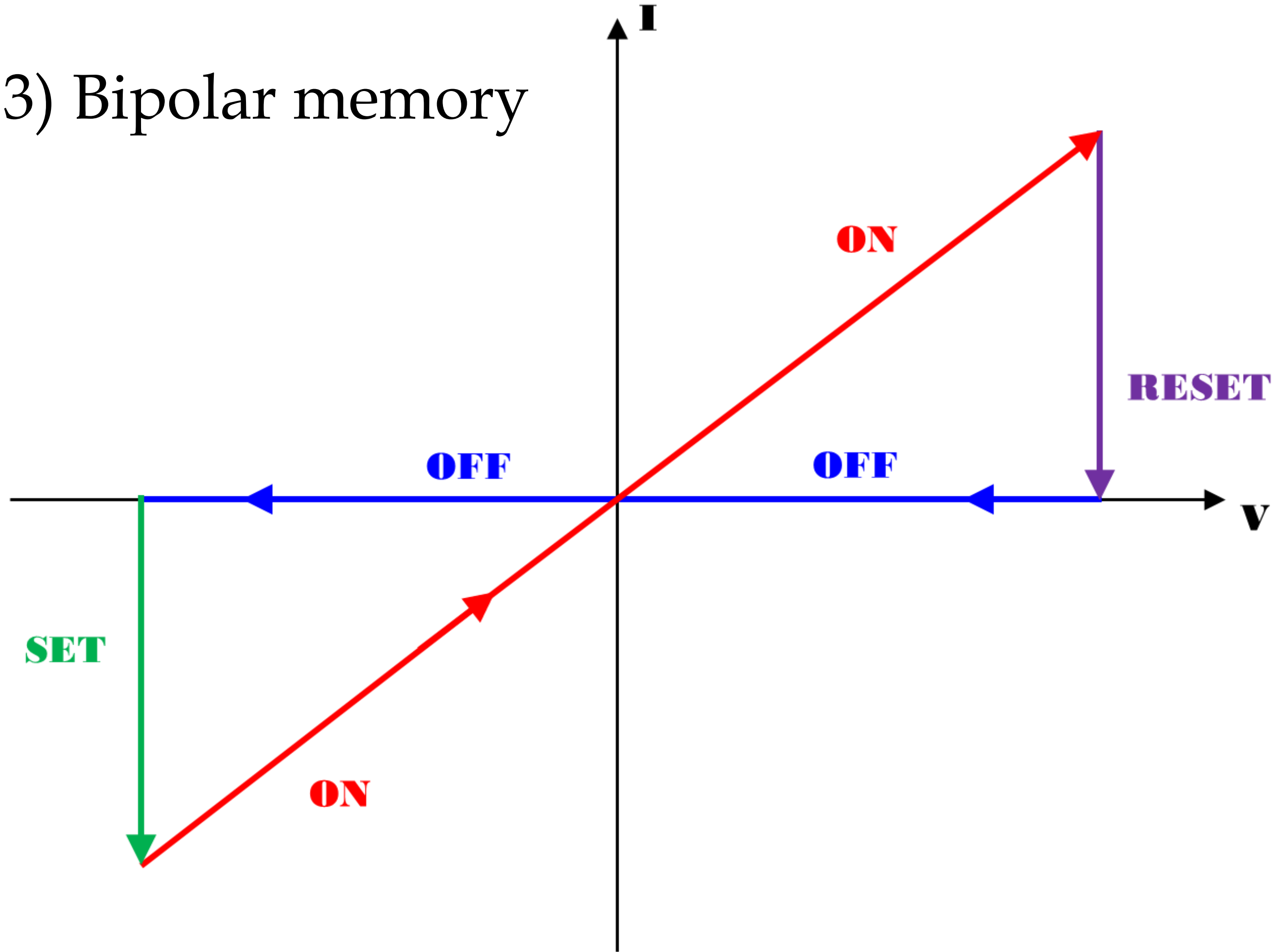
2) Unipolar memory



Organic RRAM: electrical characteristics

Typical I-V curves of **non-volatile** RRAMs

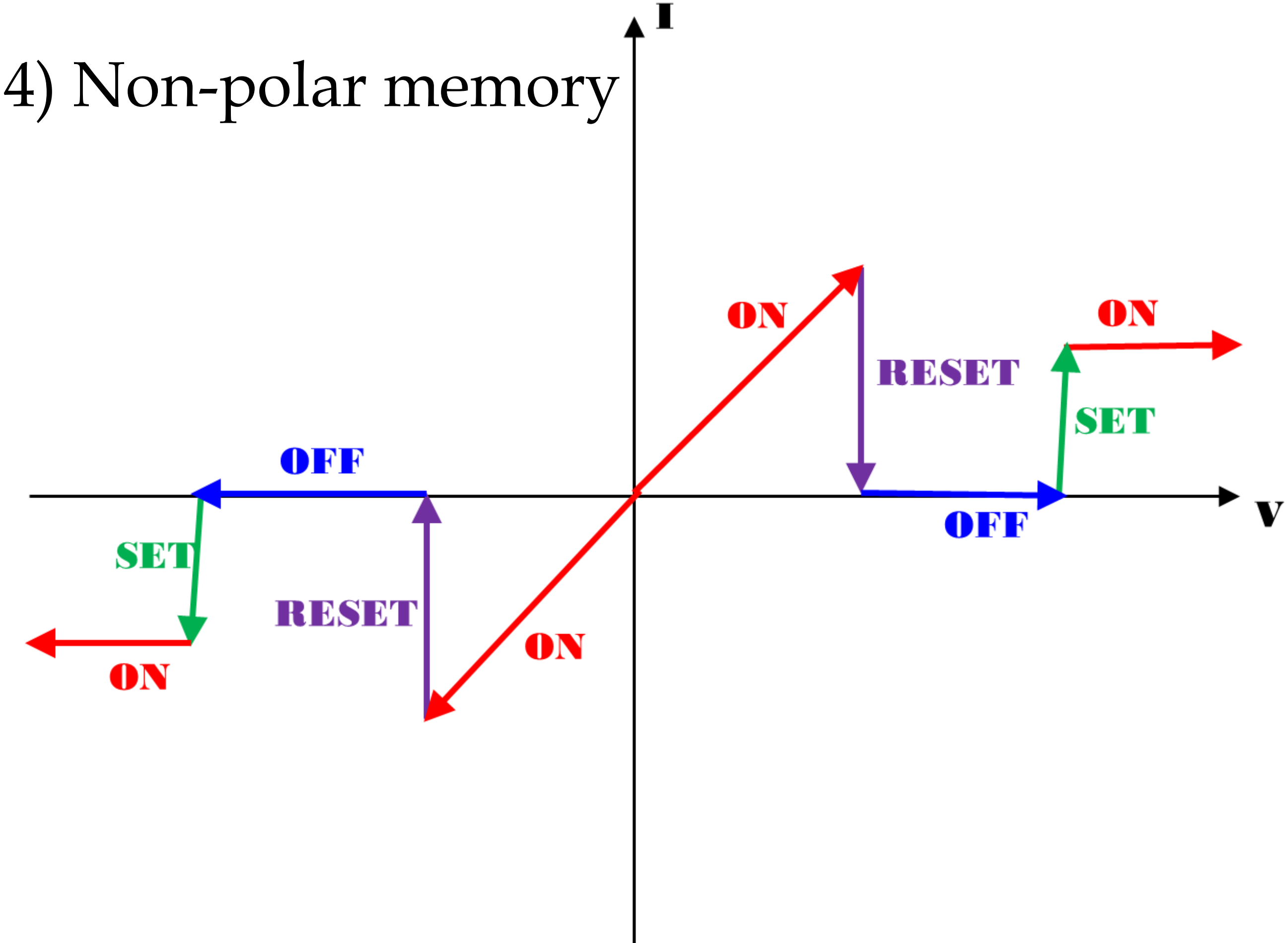
3) Bipolar memory



Organic RRAM: electrical characteristics

Typical I-V curves of **non-volatile** RRAMs

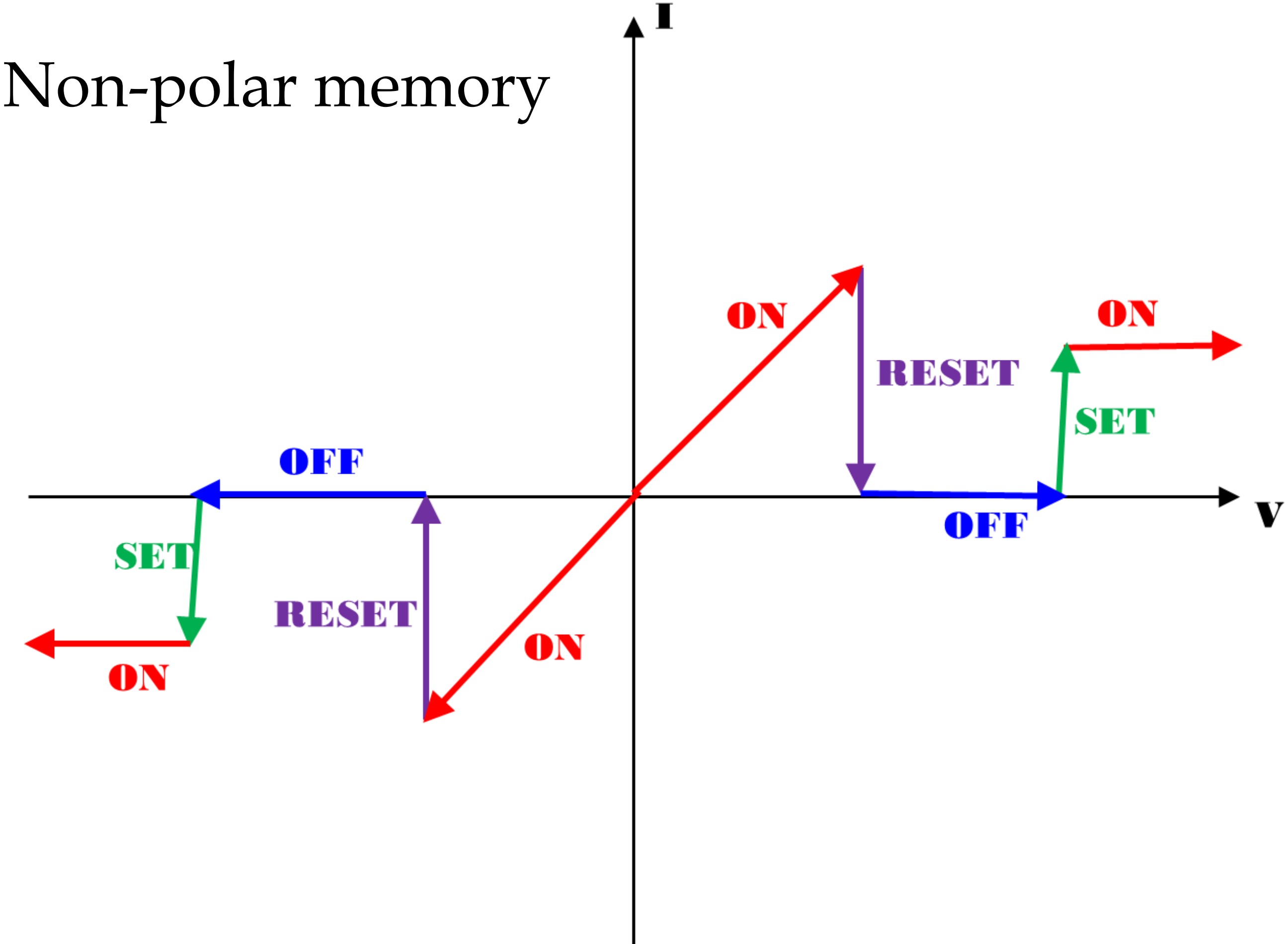
4) Non-polar memory



Organic RRAM: electrical characteristics

N-Shaped I-V characteristic: **Negative differential resistance (NDR)**

Non-polar memory



Organic RRAM: electrical characteristics

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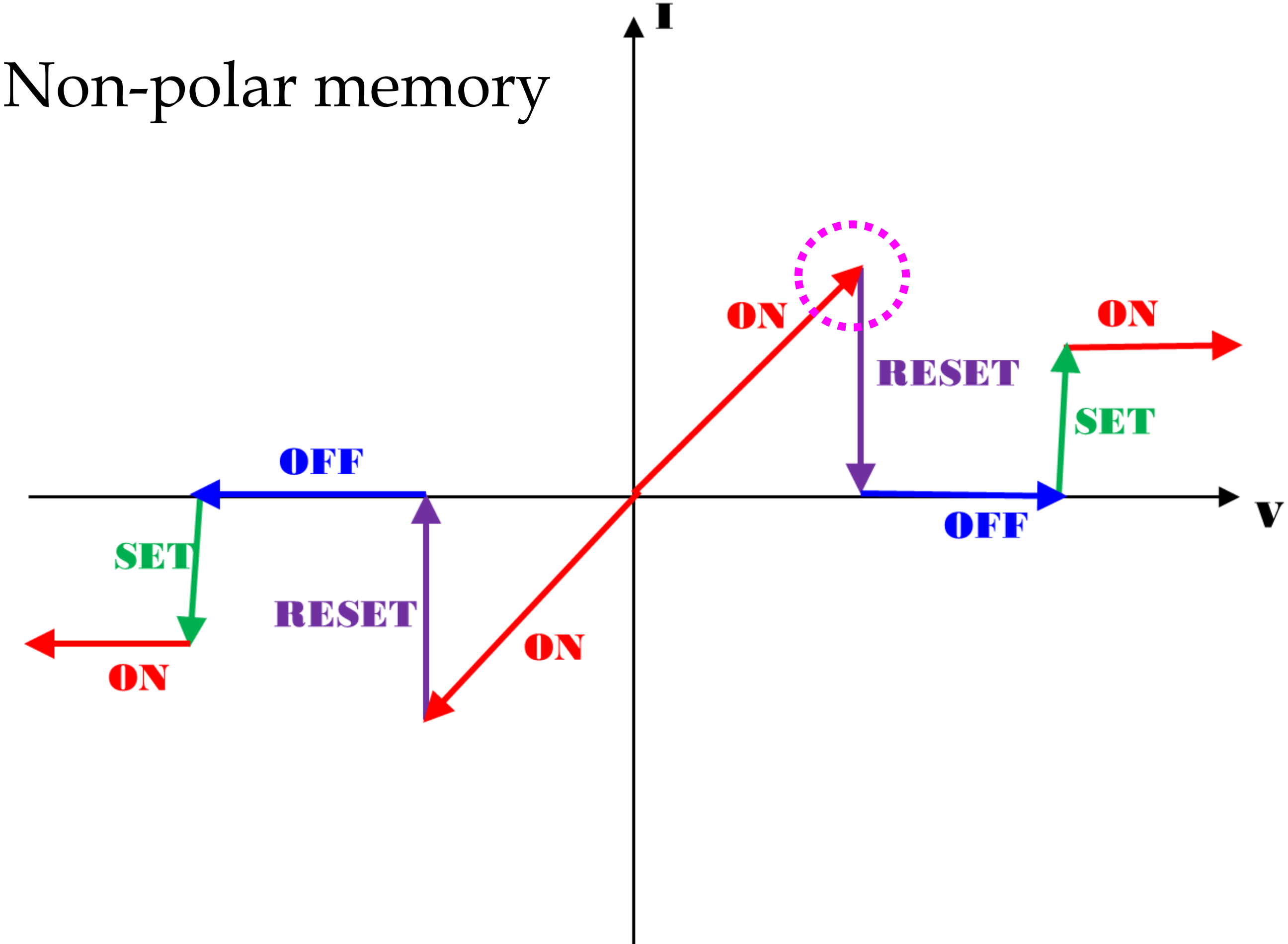

Organic RRAM: electrical characteristics

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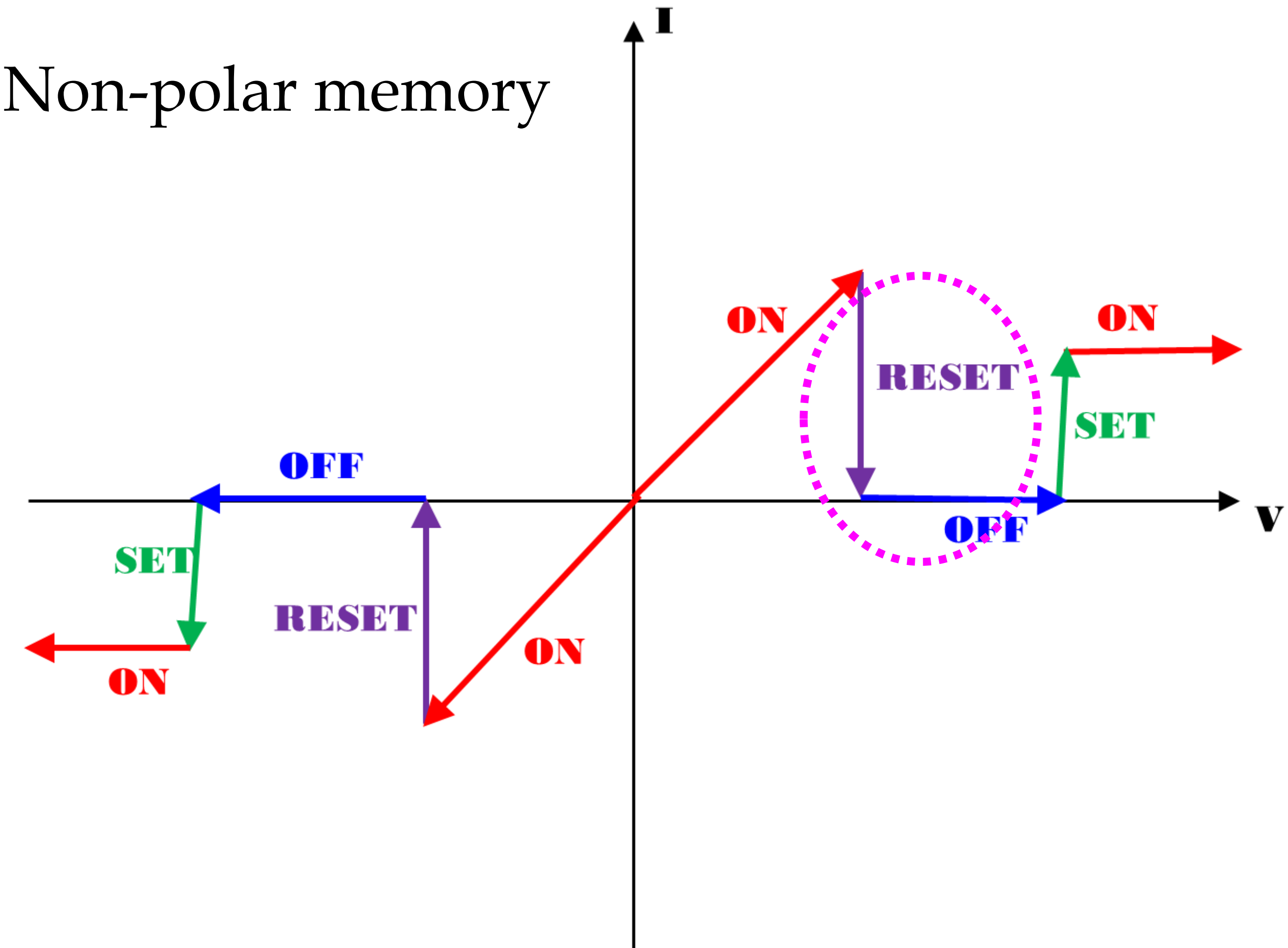

Organic RRAM: electrical characteristics

N-Shaped I-V characteristic: **Negative differential resistance (NDR)**

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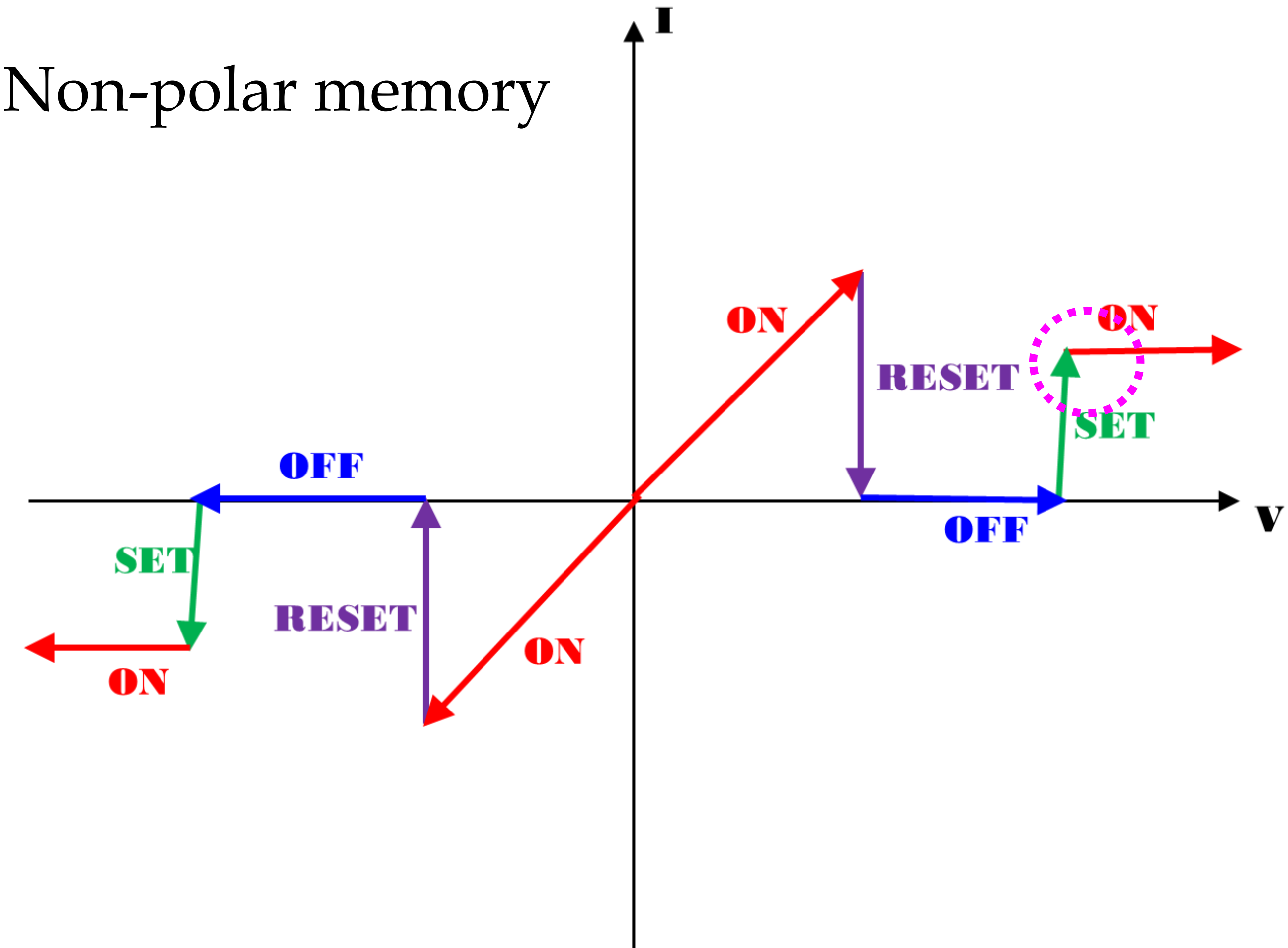
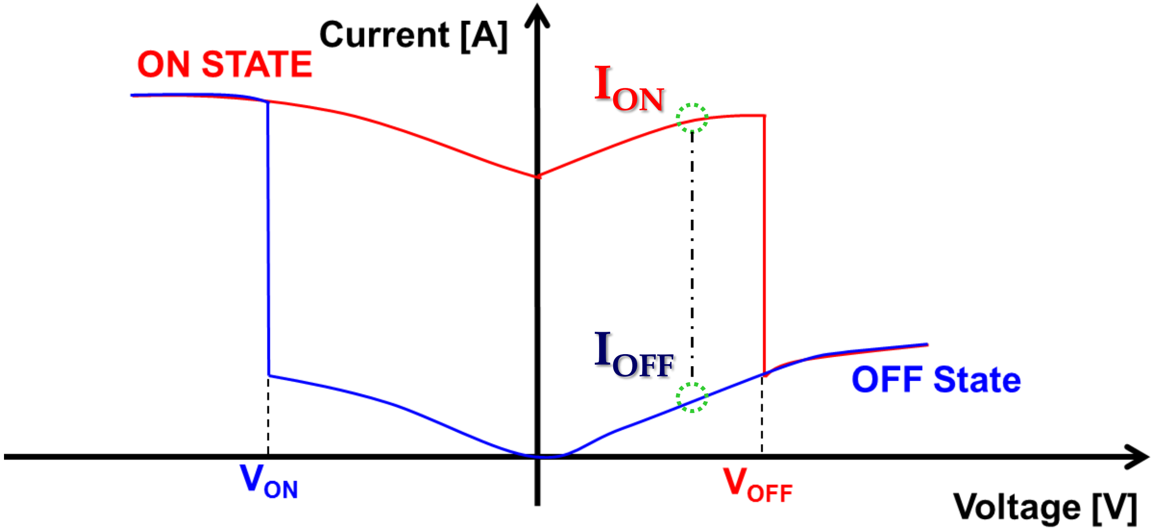


Organic RRAM: basic parameters

- **Operating voltage (writing , reading and erasing)**
- **ON/OFF current ratio (I_{ON}/I_{OFF}):** ratio between the current in the ON state at a voltage V and the current in the OFF state at the same voltage V



- **Retention time**: period of time the memory can retain data

Organic RRAM: conduction mechanisms

- RRAM is based on conductivity change of materials in response to the applied electric field (*non-ohmic conductivity*)
- Since conductivity is essentially a product of carrier concentration and charge mobility, non-ohmic conductivity can be induced by
  - a change in carrier concentration
  - a change in charge mobility
  - a change in both
- The electrical conduction mechanism in polymers is much more complex than in ordered inorganic materials: it cannot be explained adequately on the basis of band theory, as most polymers are amorphous in nature
- A substantial amount of research has been dedicated to understanding the switching phenomena associated with these devices
- Although the subject is still controversial, researchers have proposed several switching mechanisms based on theoretical simulations, experimental results and advanced analytical techniques

Organic RRAM: conduction mechanisms

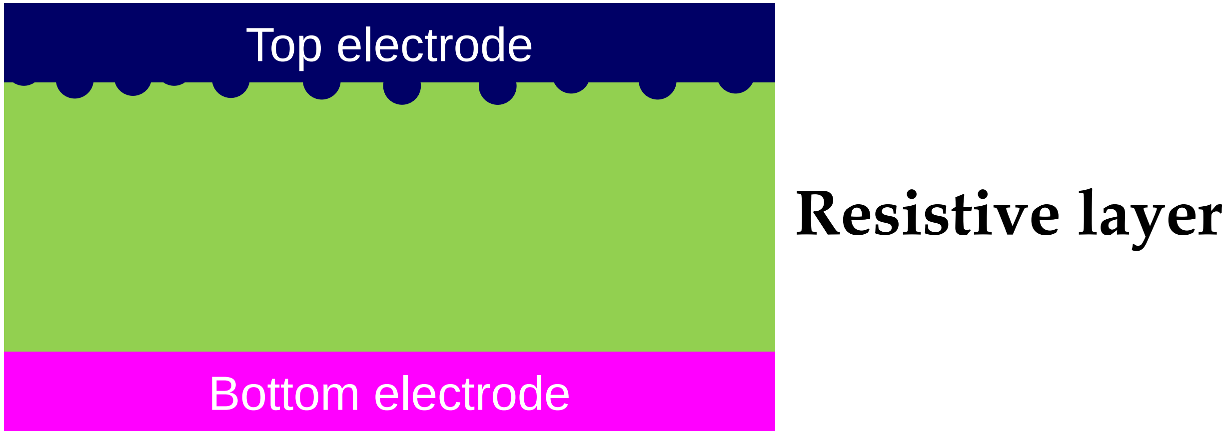
The most widely used switching mechanisms in organic resistive memory devices:

- ✓ Filamentary conduction
- ✓ Space charge and traps
- ✓ Charge transfer
- ✓ Conformational change
- ✓ Ion conduction

Organic RRAM: Filamentary conduction

- ON state current is highly localized to a small fraction of the device area
- Electrical switching is a consequence of the formation, rupture and reformation of these filaments

OFF State



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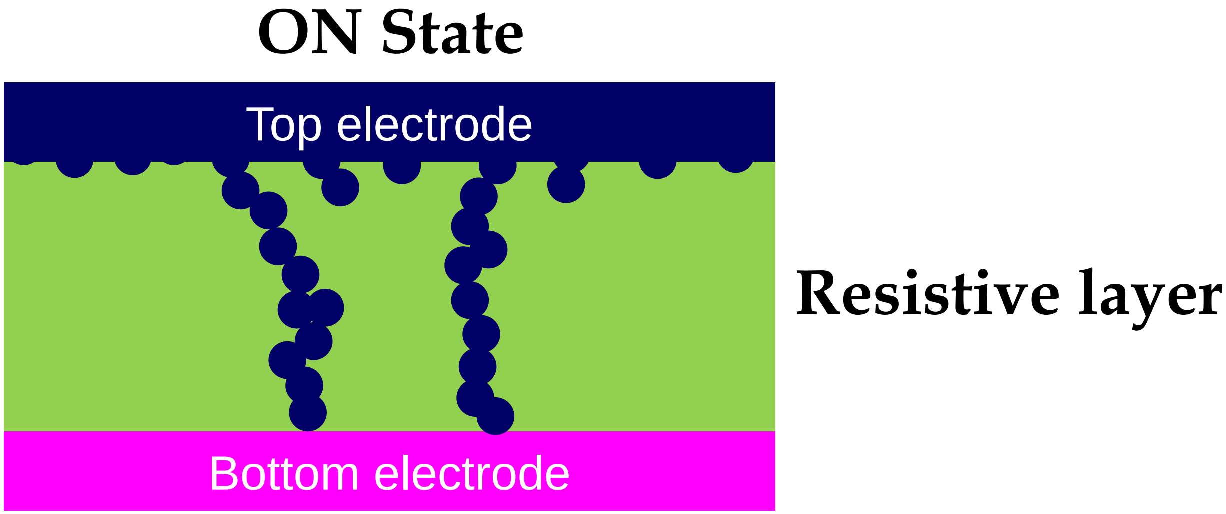

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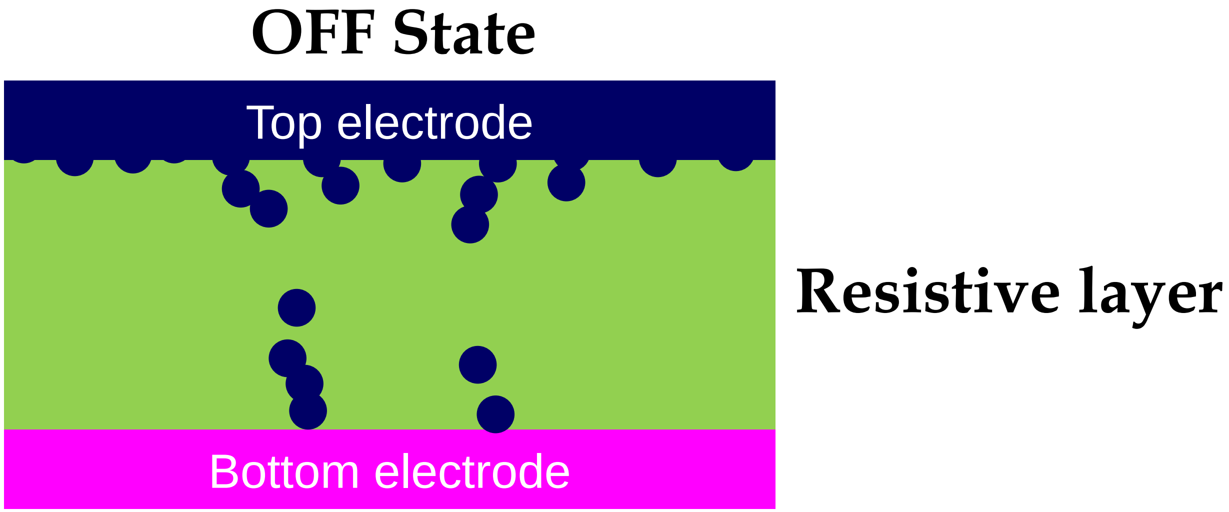
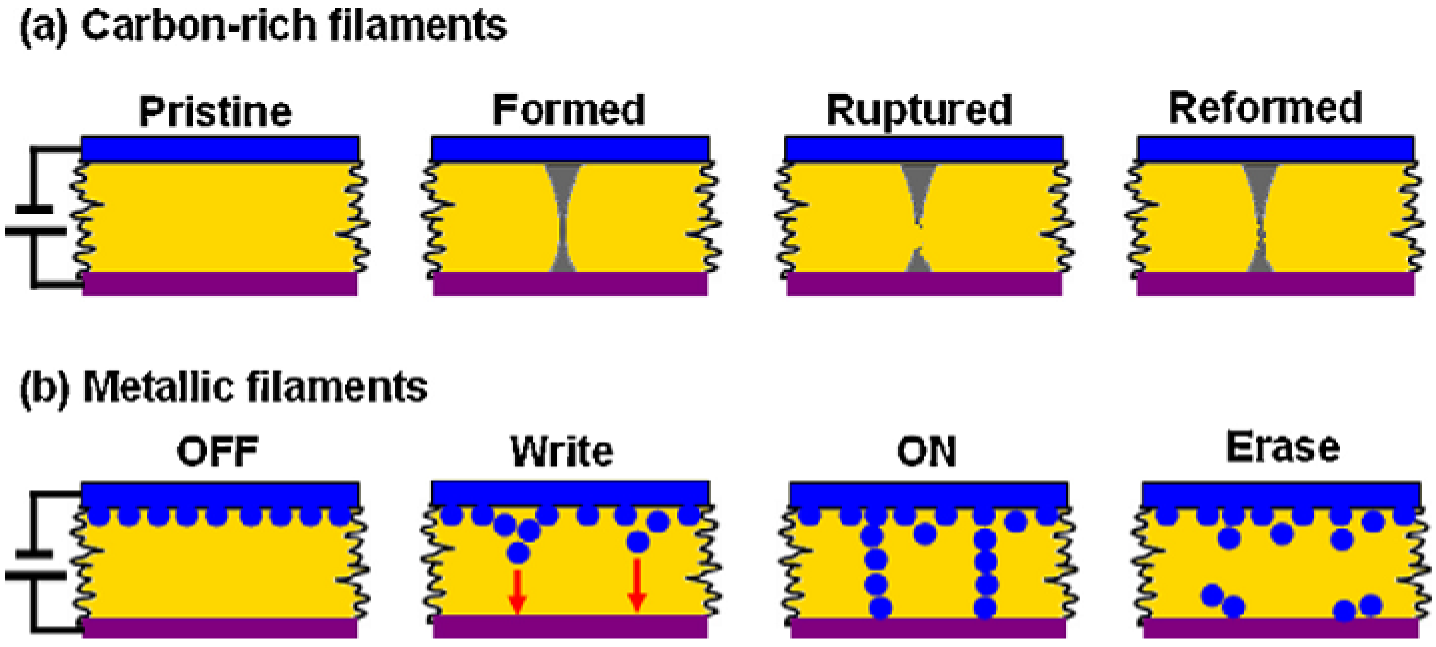


Organic RRAM: Filamentary conduction

- It is difficult to elucidate the nature of the localized conductive paths
- Two kinds of filamentary conduction have been conceptually suggested

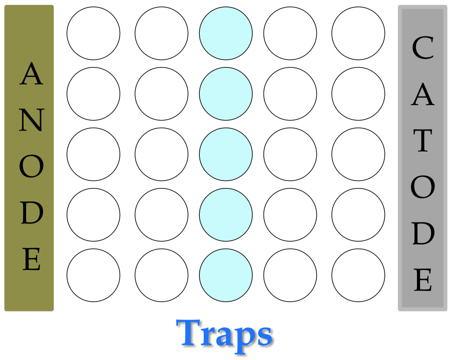


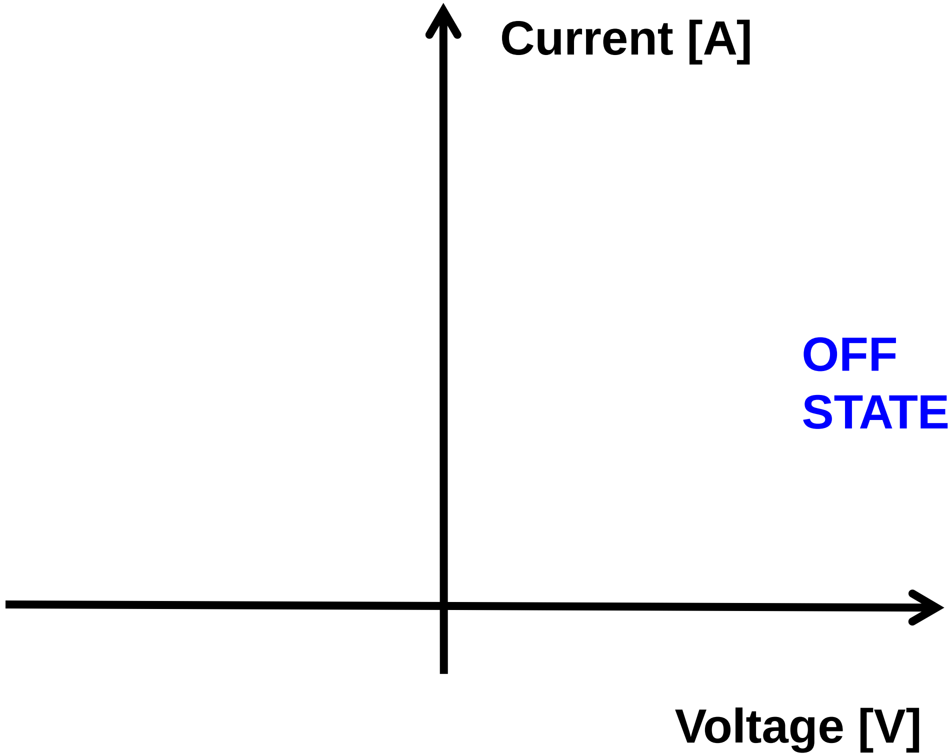
Organic RRAM: Space charge and traps

- Electrical switching behaviors of some organic materials has been reported to be associated with **space charges and traps**
- **Space charges** in materials may arise from several sources:
  - injection of electrons or holes from the electrode
  - presence of ionized dopants in interfacial depletion regions
  - accumulation of mobile ions at the electrodes interfaces
- **Traps** may be present in the bulk material or at interfaces where they will act to reduce carrier mobility. When the traps are located at interfaces, they may also affect the injection of charges into a material

Organic RRAM: Space charge and traps

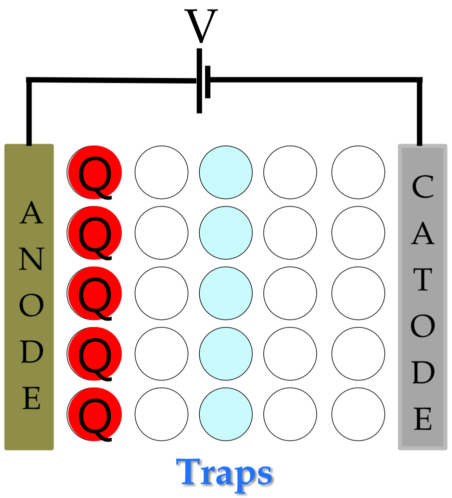
Charge trapping process

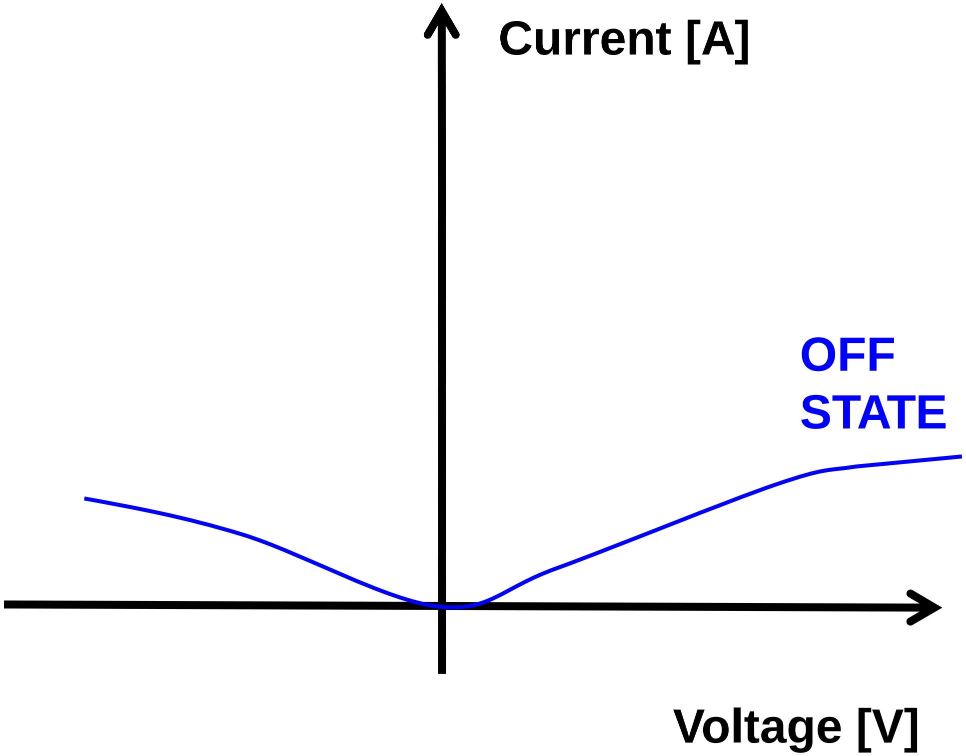




Organic RRAM: Space charge and traps

Charge trapping process

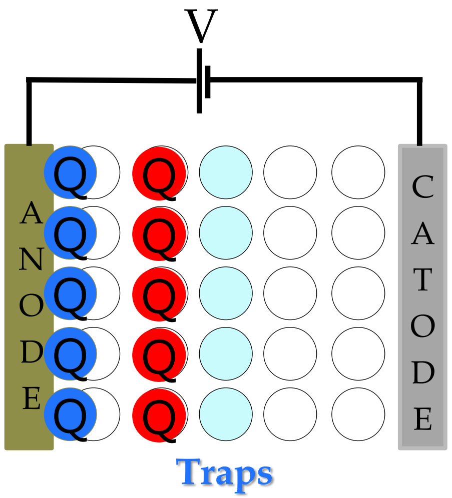


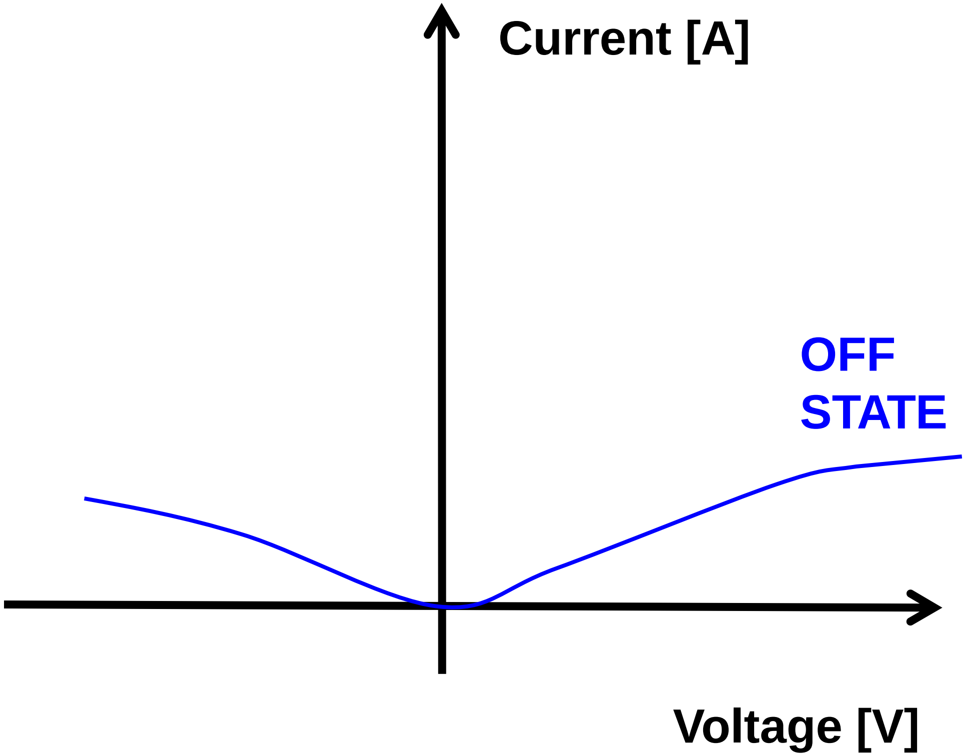


Carrier generation near the anode

Organic RRAM: Space charge and traps

Charge trapping process

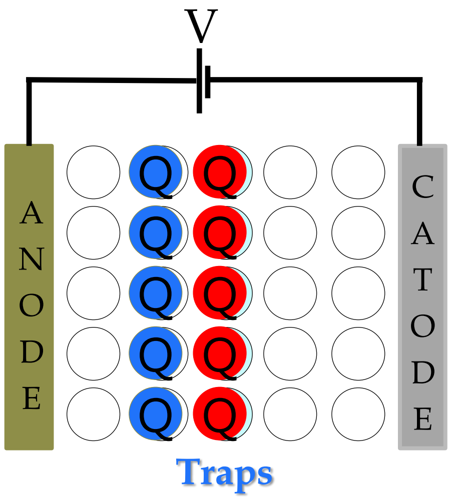


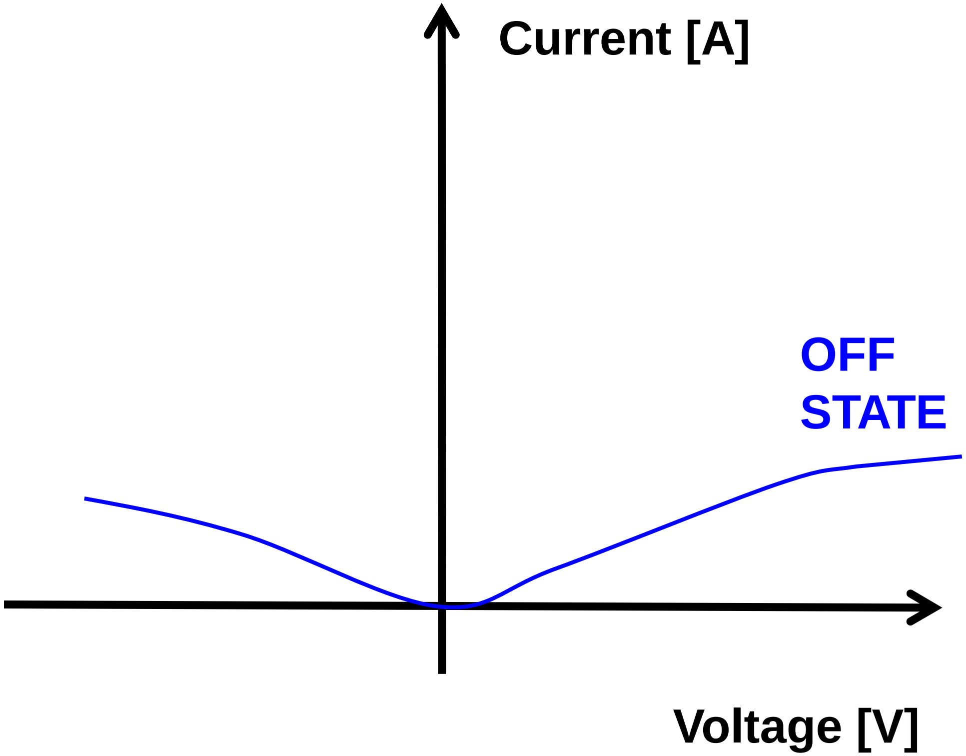


Accumulation of space charge and redistribution of the electric field

Organic RRAM: Space charge and traps

Charge trapping process

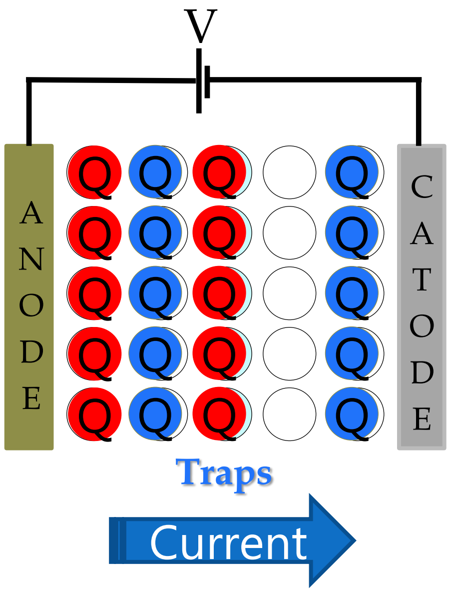


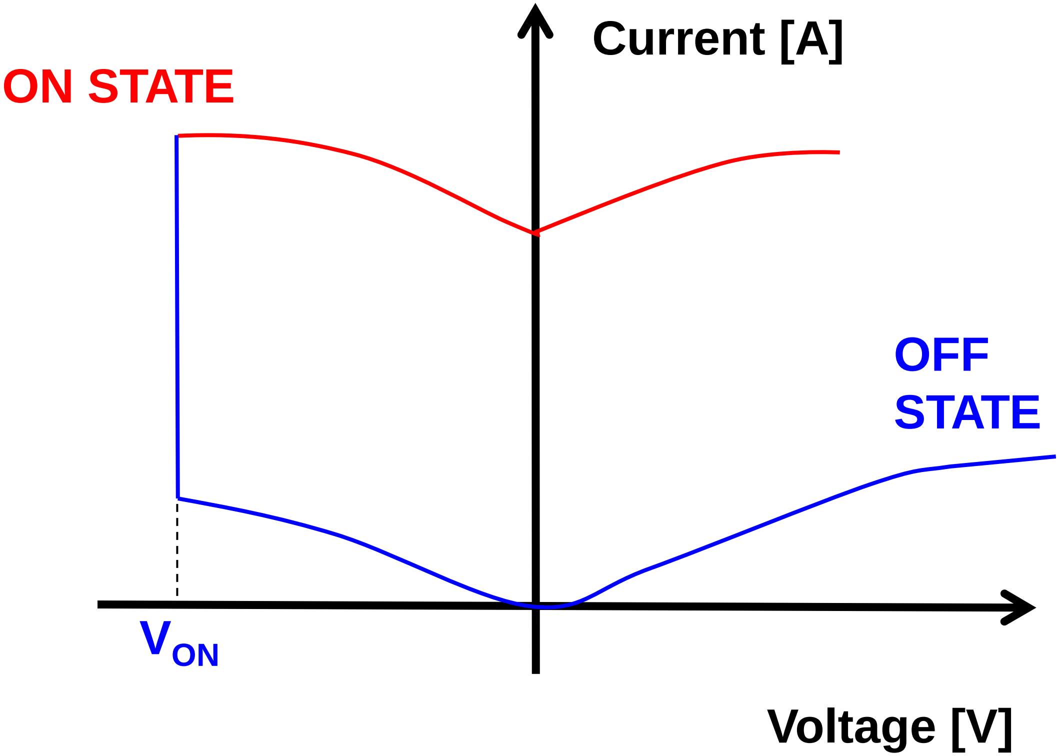


At near the turn-on voltage, the generated carriers fill some of the charge traps

Organic RRAM: Space charge and traps

Charge trapping process



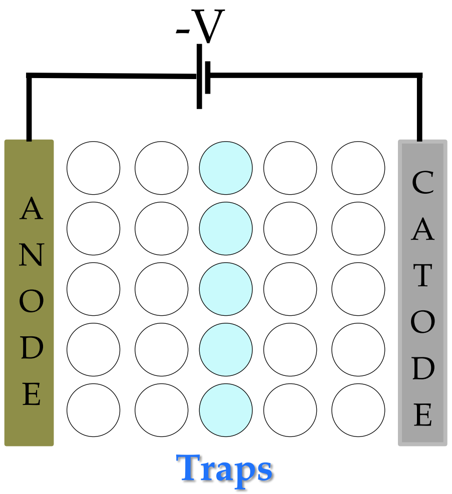


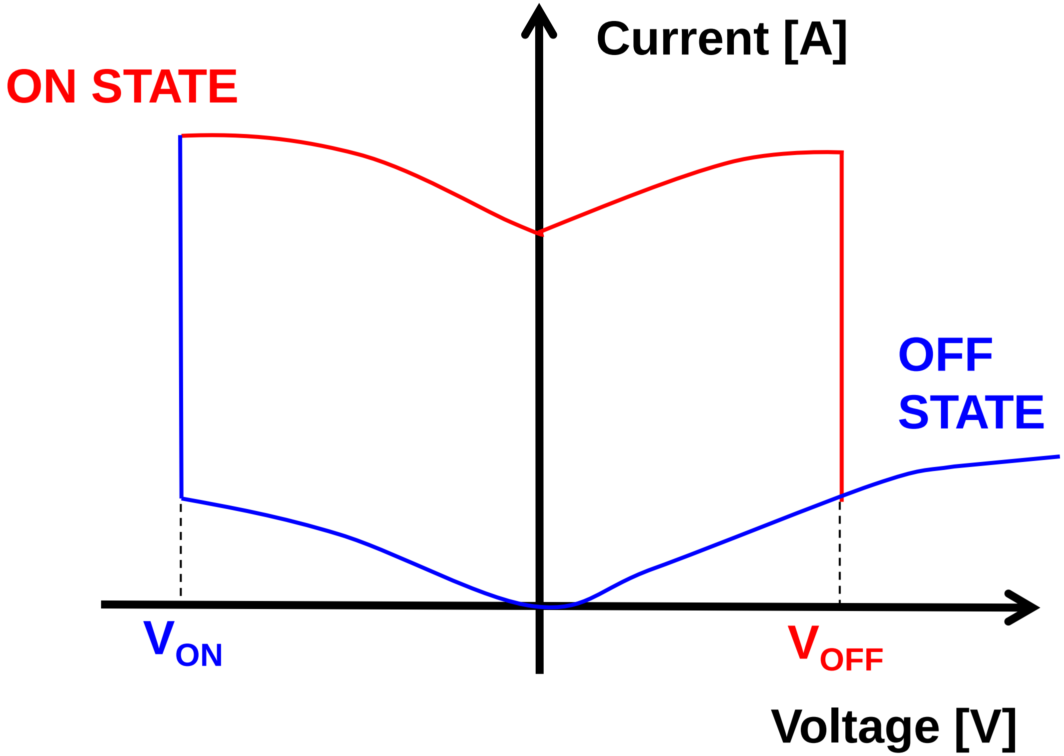
Also the cathode becomes an carrier-injecting contact , enhancing carrier concentration and mobility.

The current increases to switch the device in the ON state.

Organic RRAM: Space charge and traps

Charge detrapping process





A reversed voltage pulse causes detrapping of the filled traps

Progress in organic resistive memories

1968 *[Gregor, Thin Solid Films, 2(3):235–246, 1968]*

- Metal – insulator – metal (MIM) sandwich
- Resistance changes of several orders of magnitude at a voltage of 1–2 V
- Retention time in air of 30 minutes

1971 *[Carchano et al., Applied Physics Letters, 19(10):414–415, 1971]*

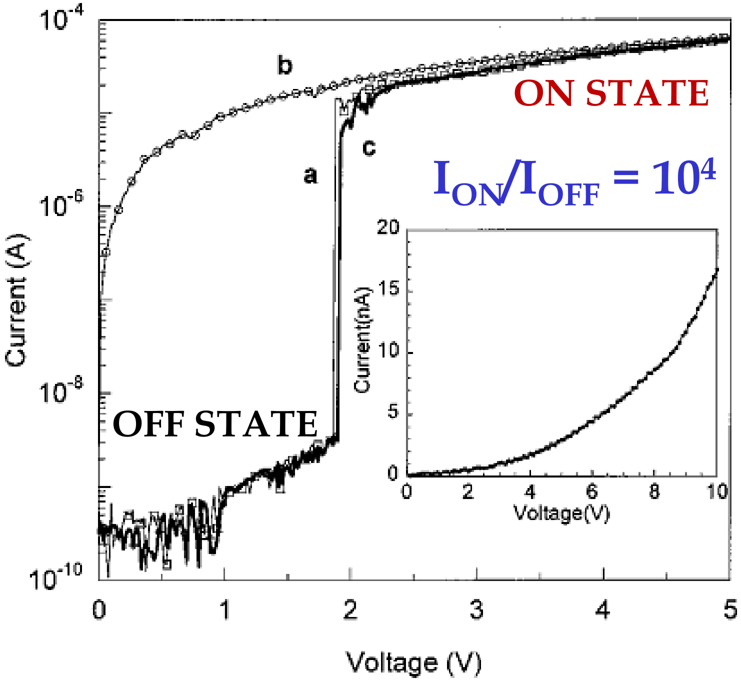
- Reproducible bistable switching in Au-Polymer-Au junctions
- Resistance ratio > 10^7

These very early results already reveal the **experimental difficulties** associated with the **irreproducible behaviors**.
For this reason, investigation has continued over the succeeding three decades but with relatively little attention, accelerating only in recent years.

Progress in organic resistive memories

2002

- Structures first proposed by the Yang group at the University of California: an **organic/metal/organic**, triple-layer structure interposed between an anode and a cathode

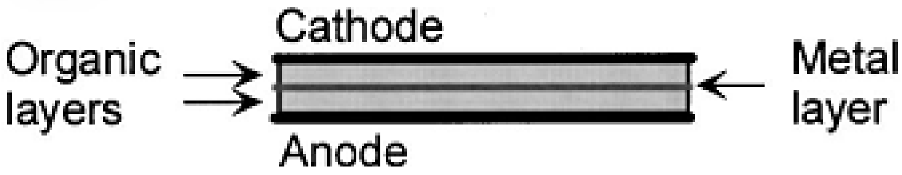


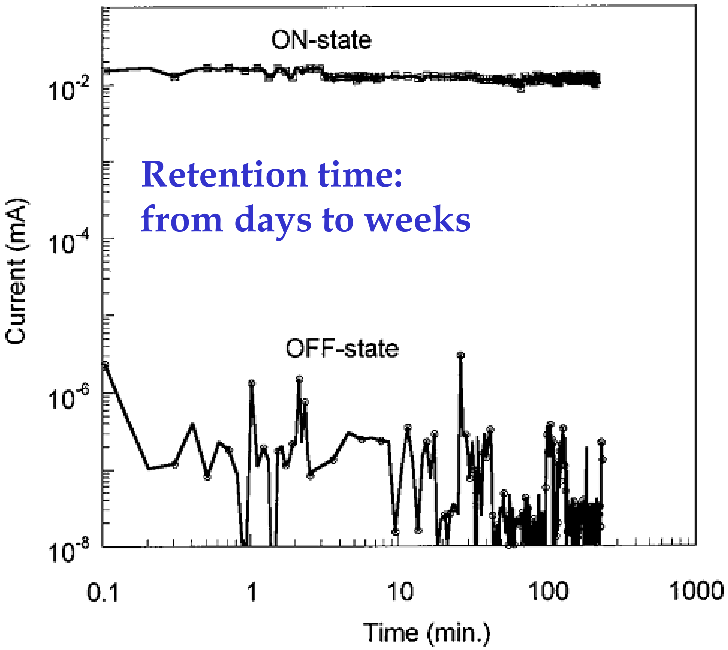
ON STATE

$I_{ON}/I_{OFF} = 10^4$

OFF STATE

L. P. Ma, J. Liu, and Y. Yang, Appl. Phys. Lett. ***2002****, 80, 2997*



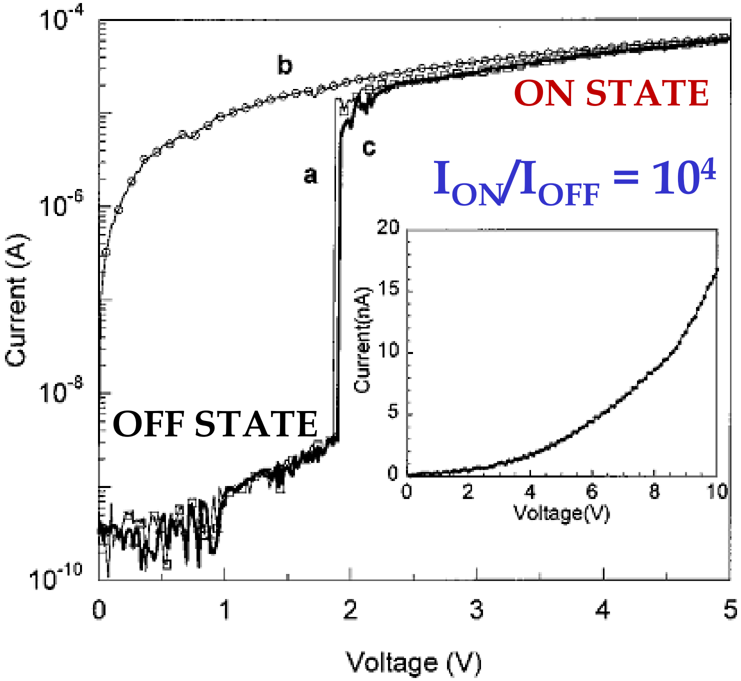


Retention time:
from days to weeks

Progress in organic resistive memories

2002

As regard the mechanism behind the resistive switching, the authors suspected that **trapped charges in the middle metal layer** are responsible for the observed electrical bistability



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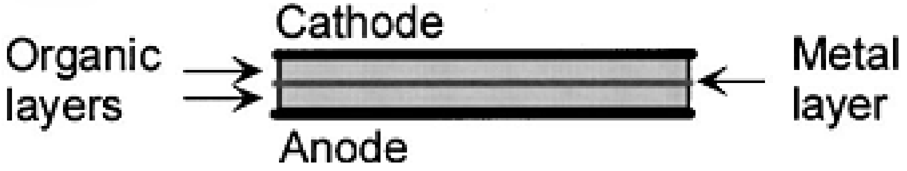
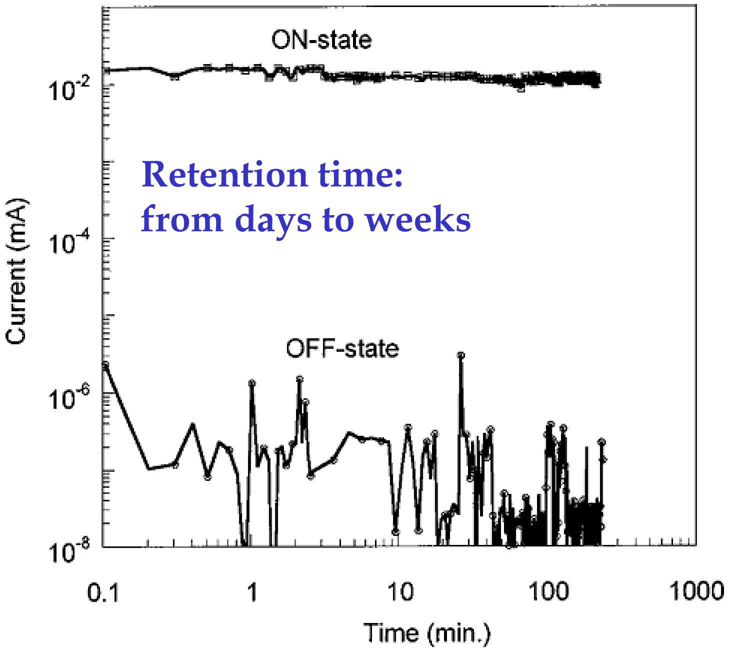


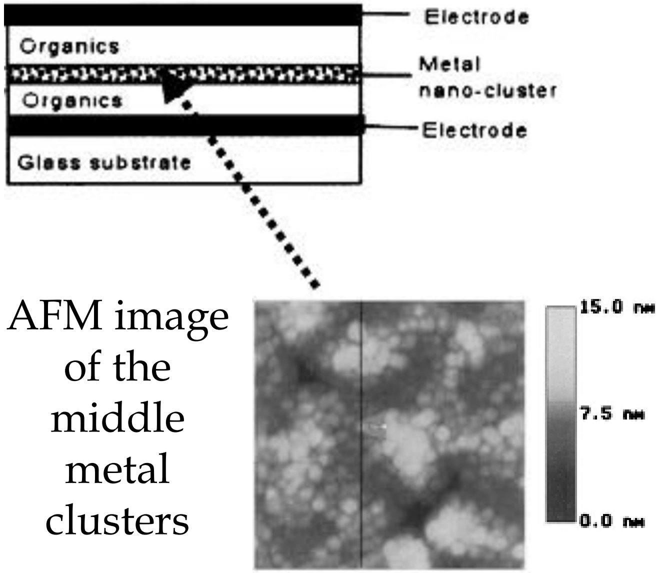


Retention time:
from days to weeks

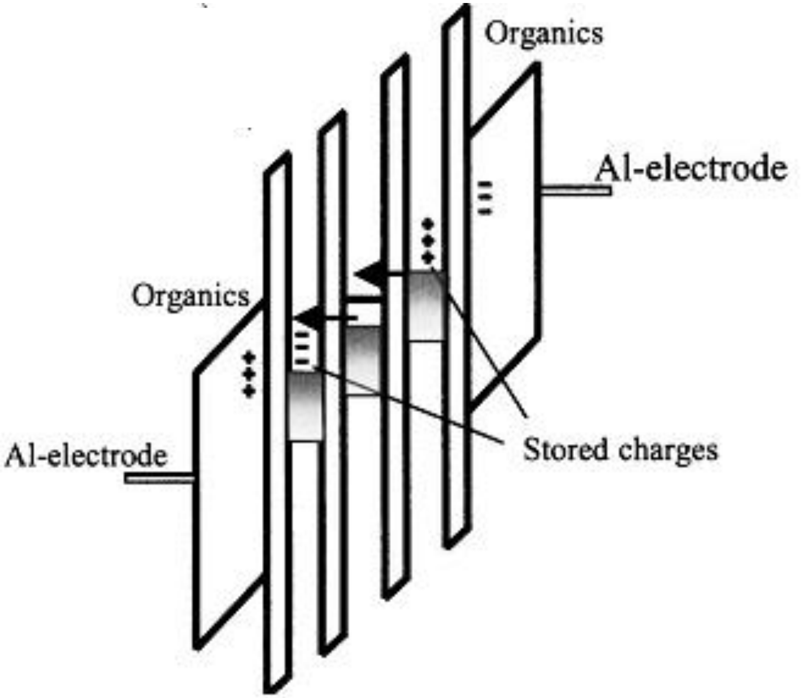
Progress in organic resistive memories

2003

- The middle metal layer for the bistable device consists mainly of partially oxidized, **small metal nanoclusters**, instead of pure metal, as previously described



AFM image of the middle metal clusters



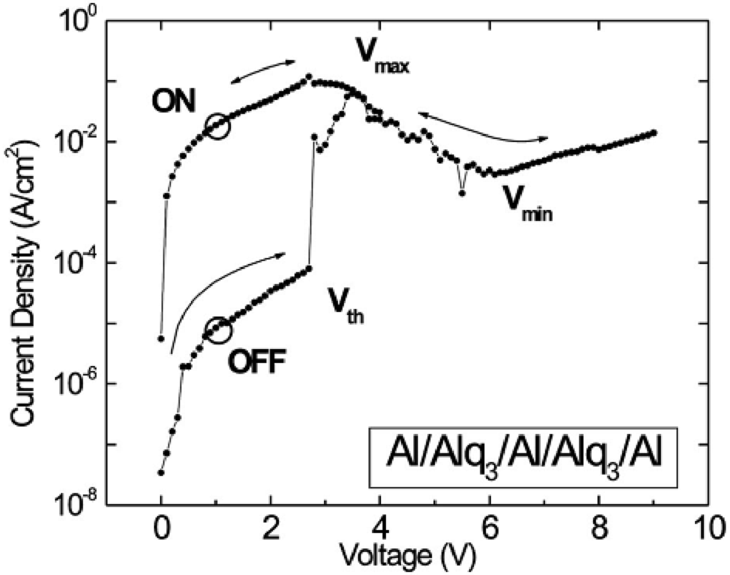
L. P. Ma, S. M. Pyo, J. Y. Ouyang, Q. F. Xu, and Y. Yang, Appl. Phys. Lett. ***2003****, 82, 1419*

Schematic energy band diagram

Progress in organic resistive memories

2004

- The **mechanisms for bistability** in these devices were thoroughly investigated by Bozano et al.
- They proposed that the resistive switching phenomenon observed in organic layers containing granular metal particles conforms to a **charge storage mechanism**
- The **mechanism** is **very general** and many other material combinations show similar behavior
- The mechanism responsible for the bistable resistance behavior of these devices is **charge trapping and space-charge** field inhibition of injection
- A **discontinuous, granular layer** is critical to the bistability of the device
- Trapping properties can be tailored by the choice of metal, the size of particles and their position in the device structure

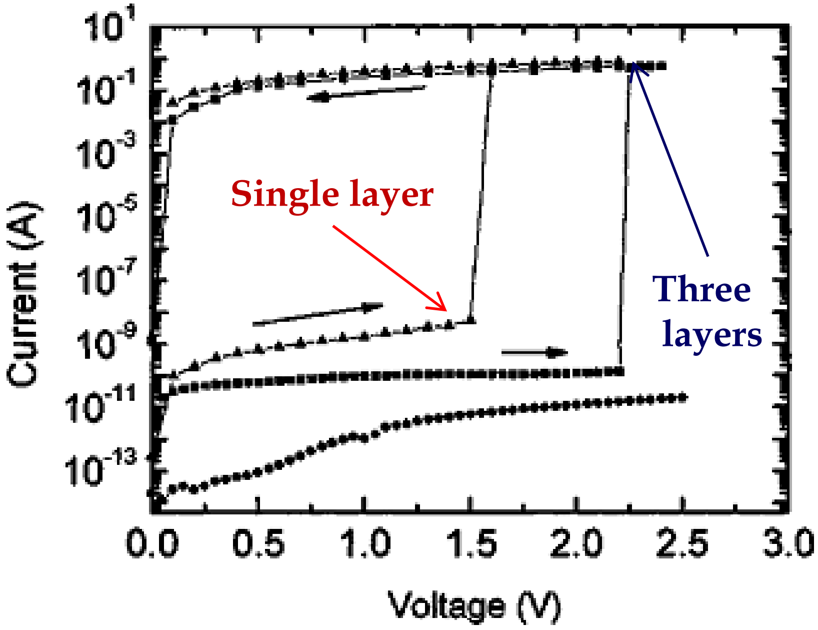


L. D. Bozano et al., Appl. Phys. Lett. 2004; 84: 607-9

Progress in organic resistive memories

2004

- At the same time Tondelier et al. report a bistable organic memory made of a **single organic layer** embedded between two electrodes
- They found that one-layer and three-layer organic bistable devices exhibit similar current–voltage characteristics



Tondelier et al., Applied Physics Letters, 85(23):5763–5765, ***2004****.*

- They observed on-state current over off-state **current ratios** as large as **10^9**
- This behavior was attributed to the inclusion of metal nanoparticles into the organic material during the top electrode evaporation for both types of devices, with **metallic filaments of nanoparticles** forming in the polymer under high electric fields, giving rise to a high conductivity ON state.

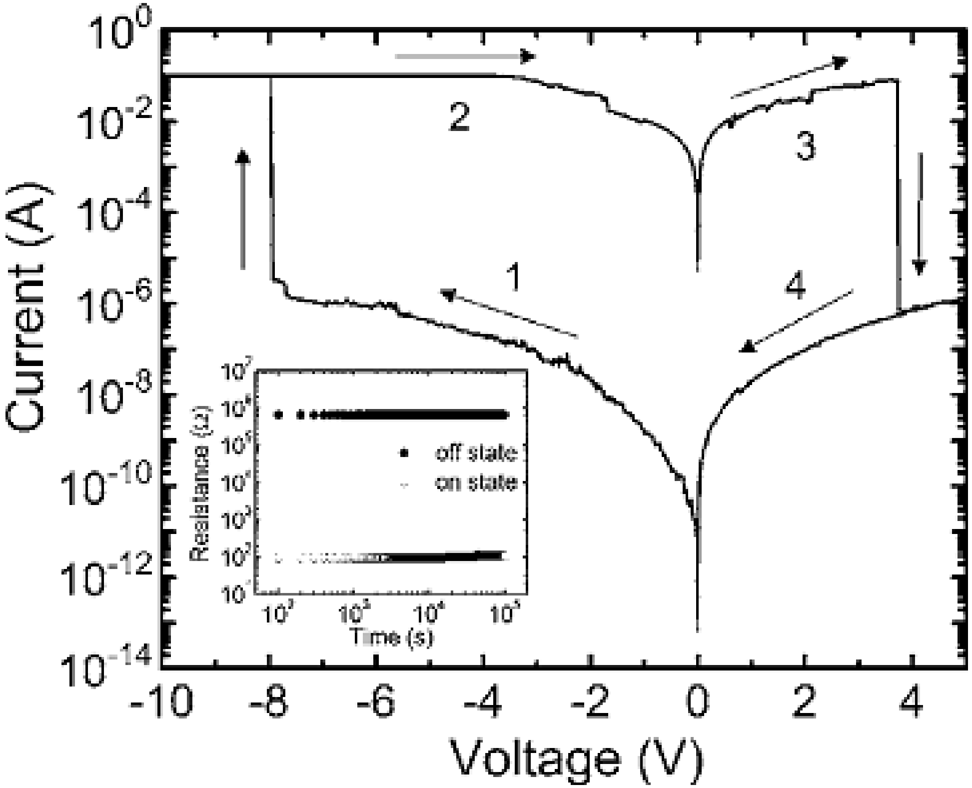
Progress in organic resistive memories

2005

- Progression in terms of perfomance were obtained by Lai et al., who demonstrated bistable resistance switching characteristics of an Aluminum/poly(N-vinylcarbazole) (PVK)/Aluminum structure

- Reproducible resistance switching
- Large **ON/OFF ratio** of **10^4**
- **Retention time** of about **10^5** sec (27 hours) in ambient conditions
- Mechanism is explained on the basis of the **filament theory**

Lai et al., Applied Physics Letters, 87(12):122101, ***2005****.*

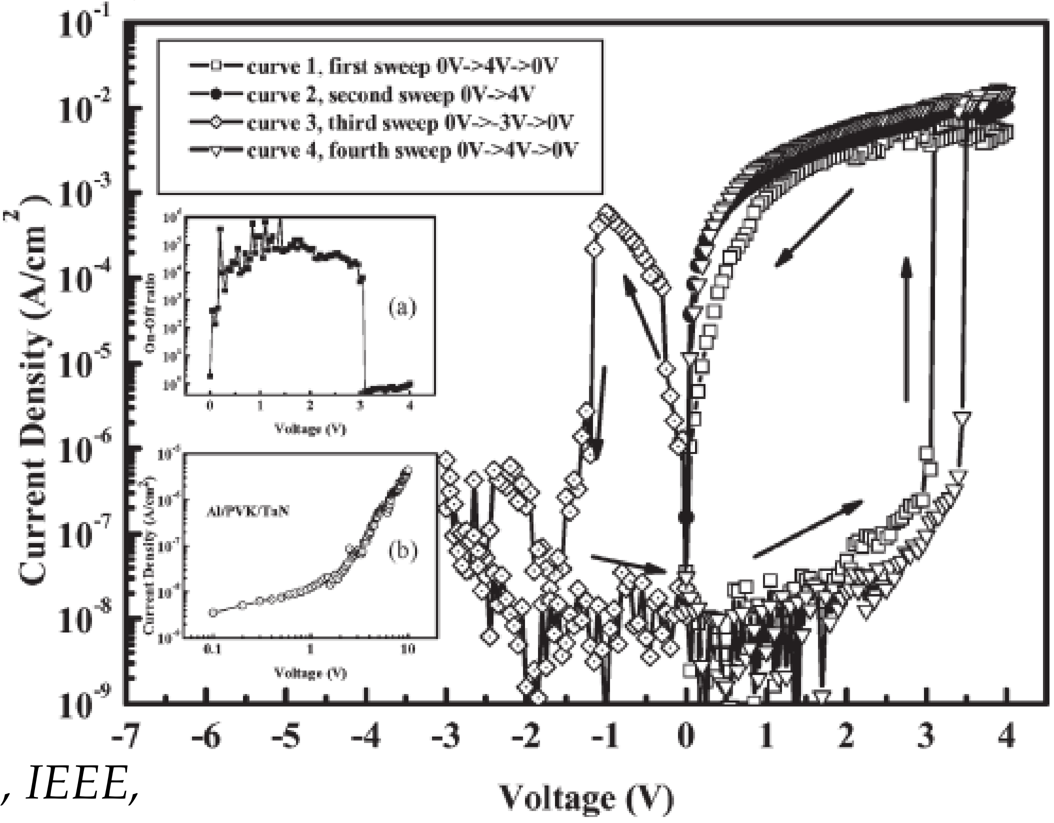


Progress in organic resistive memories

2007

- Bistable device based on PVK mixed with gold nanoparticles (GNPs), which serve as the active layer between two metal electrodes.
- Electrical bistability and memory effect are due to the incorporation of GNPs in the PVK

- PVK serves both as the matrix for GNPs and electron donor since it has a strong capability to provide electrons
- GNPs act as electron acceptors
- ON/OFF current ratio as high as 10^5



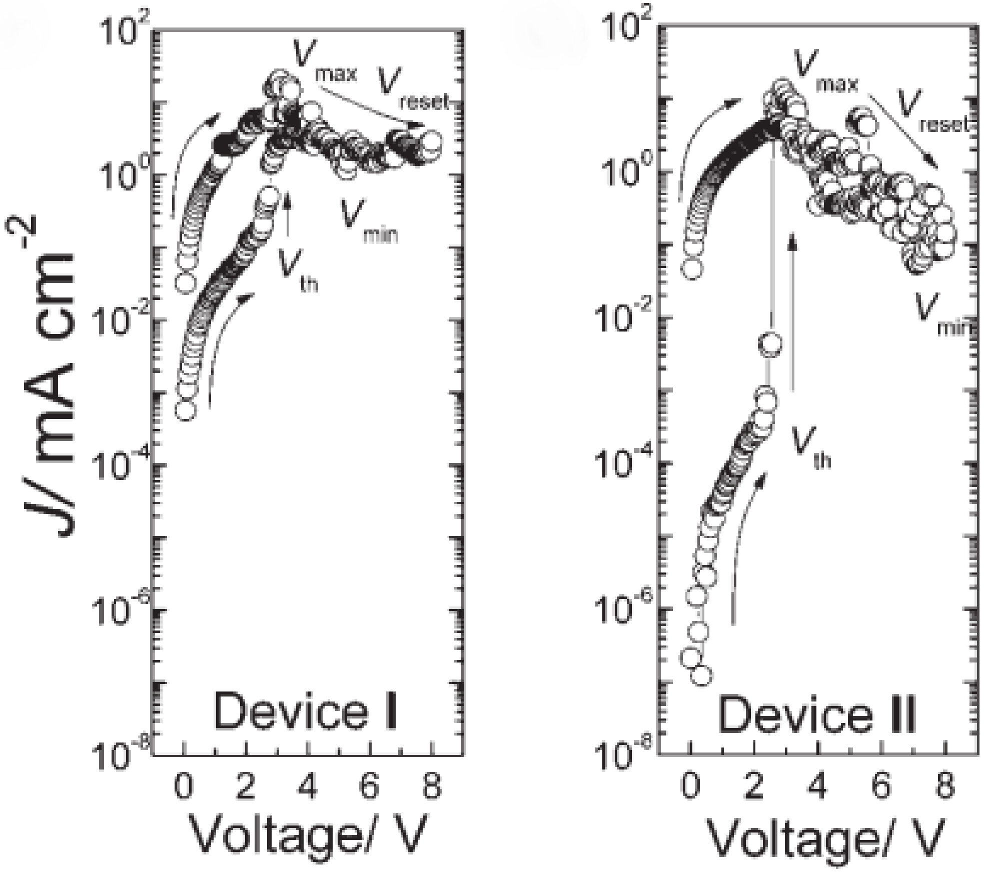
Song et al., Electron Device Letters, IEEE, 28(2):107–110, ***2007***

Progress in organic resistive memories

2008

- PVK was also used embedded between an Al electrode and ITO modified with Ag nanodots (Ag-NDs)
- Ag-NDs act as trapping sites
- **Retention time** of **3 days**
- **ON/OFF** current ratio of **10^4**

- **Device I: Without Ag-NDs**
- **Device II: With Ag-NDs**



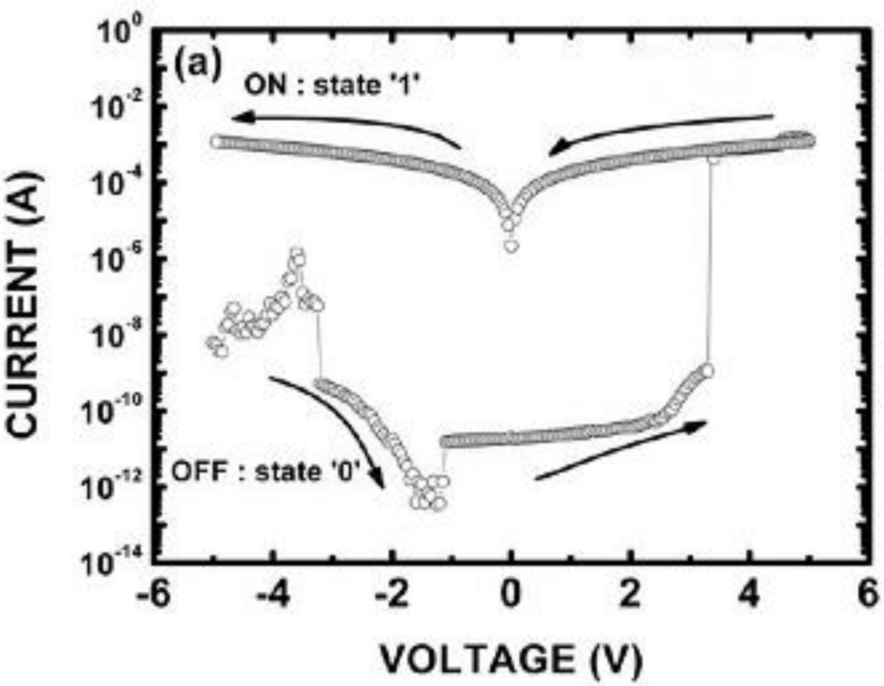
Kondo et al., Advanced Functional Materials, 18(7):1112–1118, ***2008***

Progress in organic resistive memories

2010

- Flexible non-volatile organic bistable devices fabricated with graphene sandwiched between two insulating poly(methyl methacrylate) (PMMA) polymer layer

- Bistable behavior might be attributed to conducting filaments formed in the PMMA layer at the state transition
- The graphene layer and the intrinsic trap states of PMMA act as trapping sites, which capture electrons injected from the electrode, generating a conducting filament in the PMMA layer
- **Retention time** of **10^5 sec** (27 hour) in ambient conditions
- **ON/OFF** current ratio of **10^7**



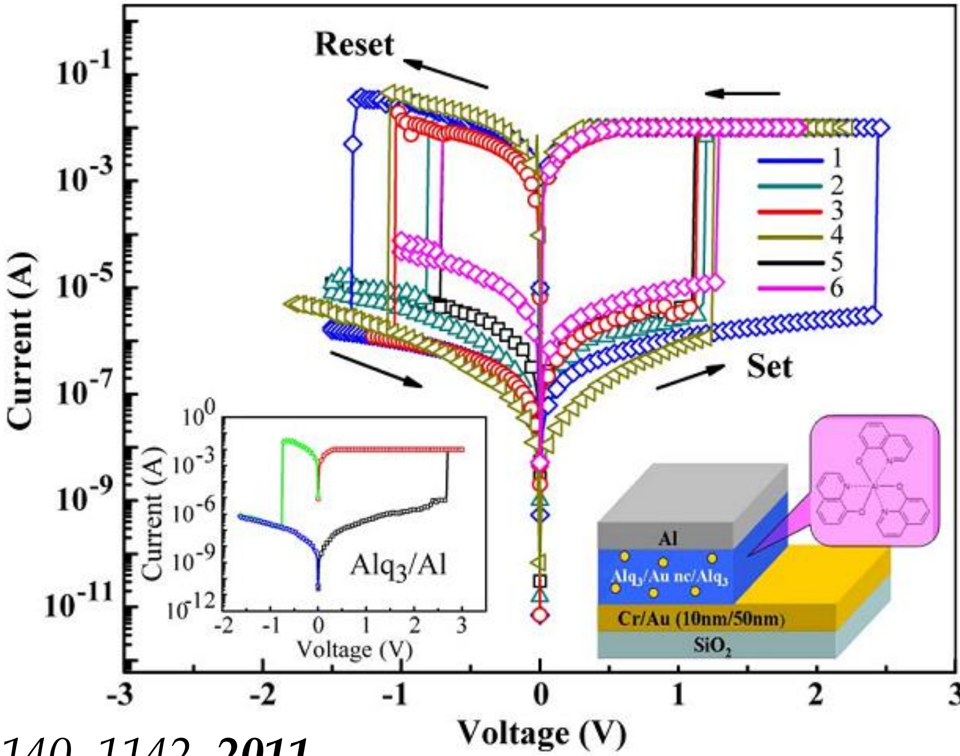
Son et al., Nano Lett. **2010**,10, 2441-2447

Progress in organic resistive memories

2011

- Organic non-volatile memories with structure Au/Alq$_3$/metal nanoparticles (Au or Al)/ Alq$_3$/Al
- Electrical characteristics of devices with gold NPs display much better performances with respect to those with aluminum NPs

- **ON/OFF** current ratio ~ **10^4**
- **Retention time ~ 4 h**
- Conduction mechanism of the devices was demonstrated to be **charge trapping:** at low voltages the conduction is dominated by intrinsic carriers of the organic material. In this region, the deep traps are mostly empty. As the bias increases, the deep traps are gradually filled, and the device turn into ON state, and a sharp increase of current density is observed.



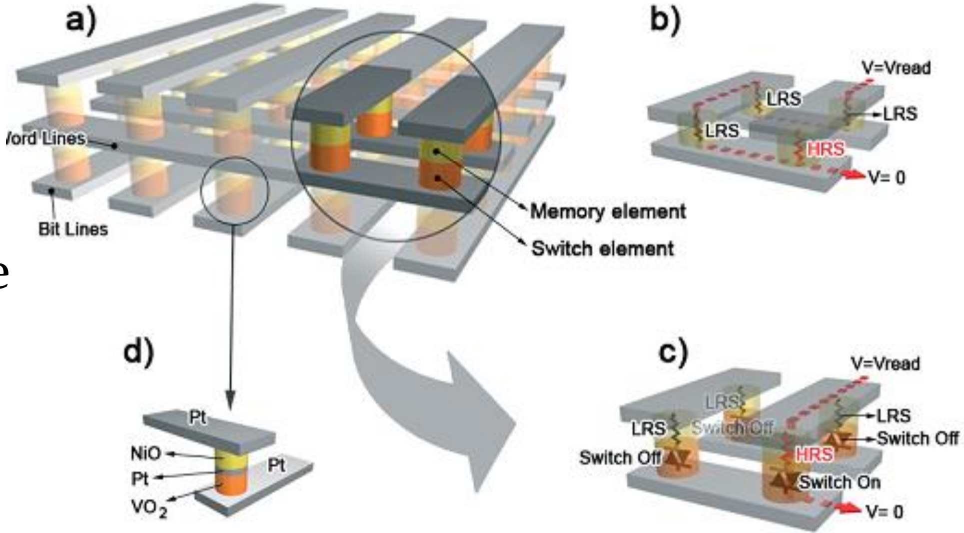
Liu et al., Electron Device Letters, IEEE, 32(8):1140–1142, ***2011****.*

Memory performance enhancement

- The switching characteristics of organic resistive memory devices are strongly influenced by the **properties of interfaces and active materials**: various approaches to control and optimize these switching properties
- **Interface between an electrode and an organic material** influences the charge injection barrier: the simplest method for modulating this interface is to **change the type of electrodes**
- Resistive switching in polymer-metal nanoparticle films can be tuned by **changing the work function of the electrode**: introducing additional layers at the metal–polymer interfaces is an effective strategy for controlling the mobility or number of charge carriers that pass through organic devices
- **Charge conduction** through a device is often strongly **governed** by the **surface morphology** of an organic film: the morphology of the organic layer should be carefully controlled to produce excellent non-volatile memory effects

Architectural concepts for advanced memory devices

- The **cross-talk phenomenon** in memory cells often occurs due to parasitic leakage paths (called **sneak paths**) through neighboring cells with low resistances in cross-bar array structures
- These phenomena disturb the reading process in selected cells, which must be eliminated in practical memory applications
- To solve the crosstalk problem, a **switching element** (diode or transistor) can be added to each memory cell
- One diode-one resistor (**1D-1R**) or one transistor-one resistor (**1T-1R**) architectures improve reading accessibility without disturbing the reading process
- **1D-1R** is **preferred** because it occupies less area and fabrication is simpler
- Different 1D-1R systems have recently been developed

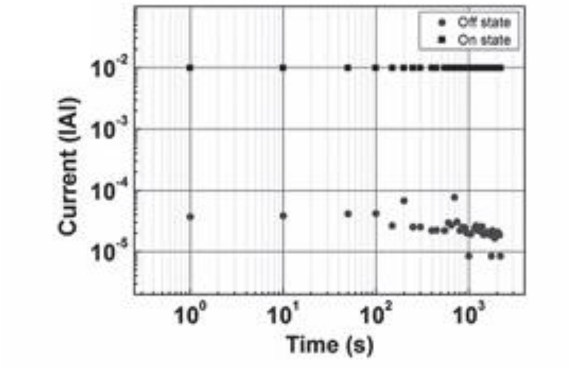


Lee et al., Adv. Mater.2007,19, 3919–3923

Organic RRAM: delopmental status

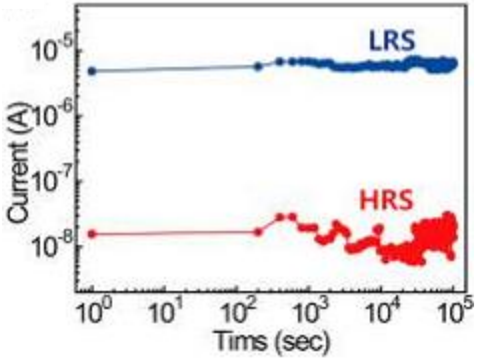
- ✓ Remarkable progress in the advancement of novel memory technologies in recent years
- ✓ Some significant challenging tasks to be resolved for practical application:
  - ➢ Complete understanding of the resistance switching mechanisms
  - ➢ Improvement of device reproducibility and reliability
  - ➢ Development of devices with long term stability for employment in ambient atmosphere
    - ❖ many devices show excellent behaviors but only in inert atmosphere
    - ❖ only few devices show a reproducible bi-stable behavior under ambient atmosphere:

Al/PS-b-PMMA:PCBM (0.05 wt%)/ITO PET



Jo et al., Macromol. Rapid Commun. 2013, 34, 355−361

Al/PS + BCNT (1.5 wt%)/Al

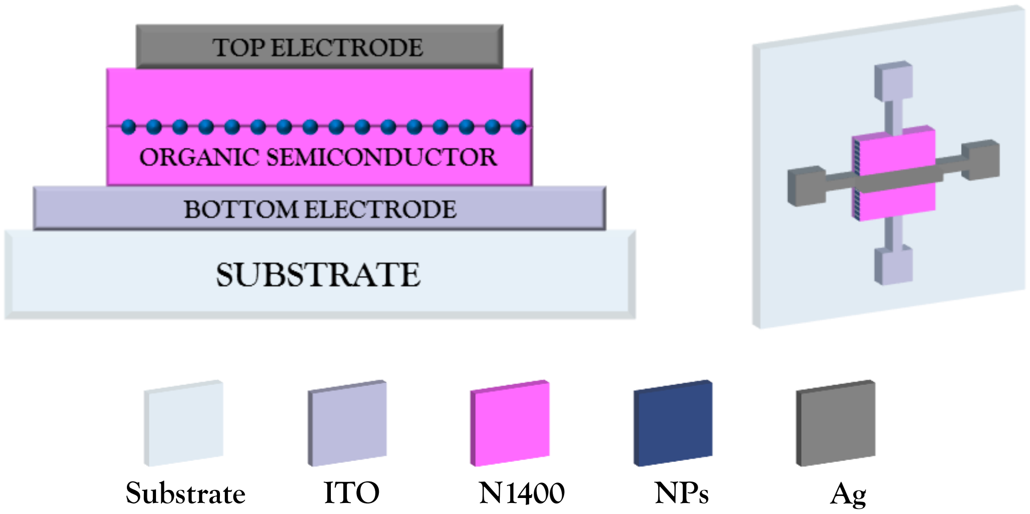


Hwang et al., Nano Lett.2012, 12, 2217−222

Maximum retention time in air in the order of 10^5 s (~1 day)

A novel organic resistive memory

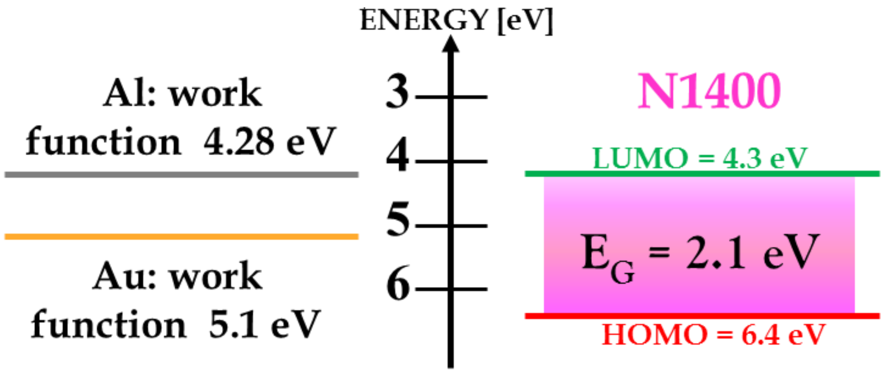
Materials and schematic

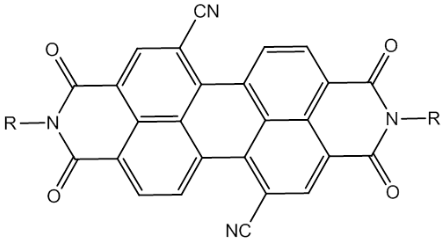


A new combination of materials

- ITO bottom electrode
  - ✓ transparent electrical conductor
  - ✓ Work function: 4.4-4.5 eV
- Ag top electrode
  - ✓ Work function: 4.26 eV
- ActivInk™ N1400 as semiconductor
  - ✓ N-type
  - ✓ Small molecule
  - ✓ Stable performances in ambient conditions

Two kinds of metal nanoparticles

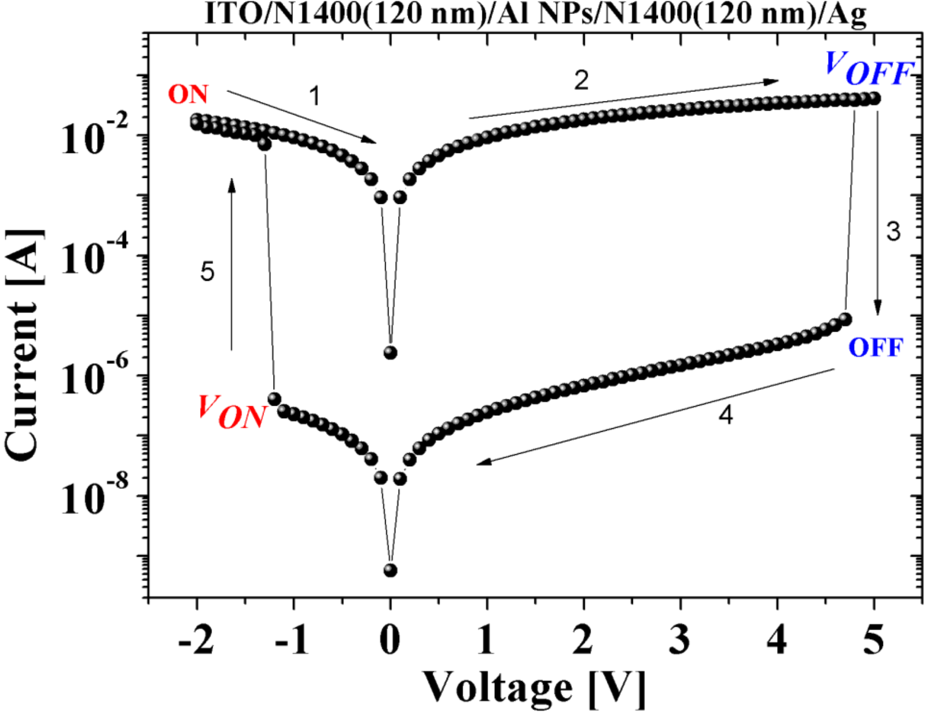




ActivInk™ N1400

Electrical characterization in air

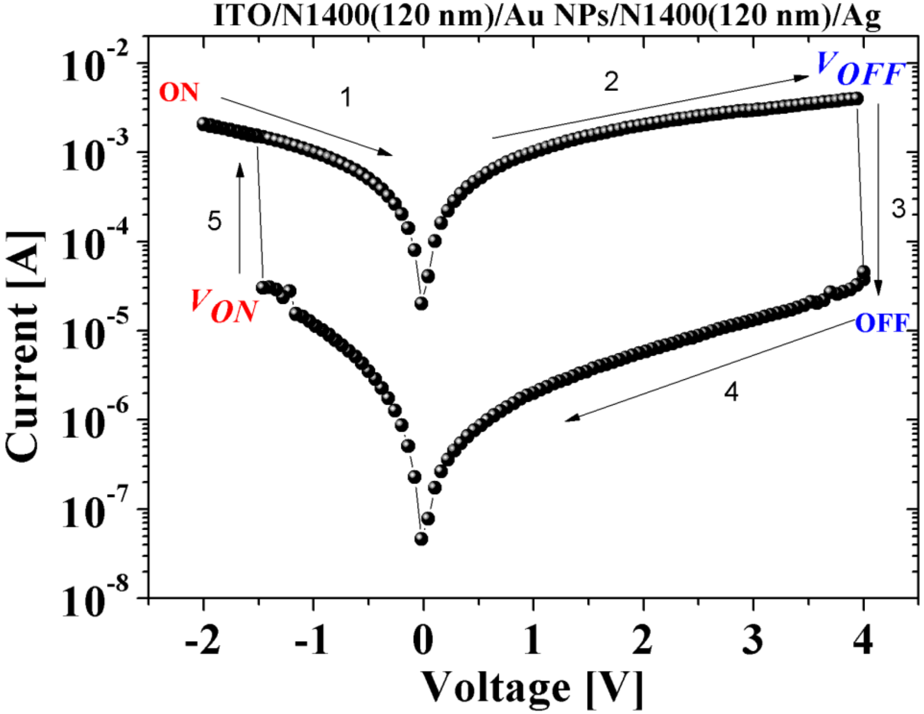
Gold Nanoparticles



ITO/N1400(120 nm)/Al NPs/N1400(120 nm)/Ag

Parameter	Average ± error
V_{WRITE} [V]	-1.6± 0.4
V_{ERASE} [V]	+3.1 ± 0.6
I_{ON}/I_{OFF}	$(4 \pm 1)\cdot 10^3$

Aluminum Nanoparticles



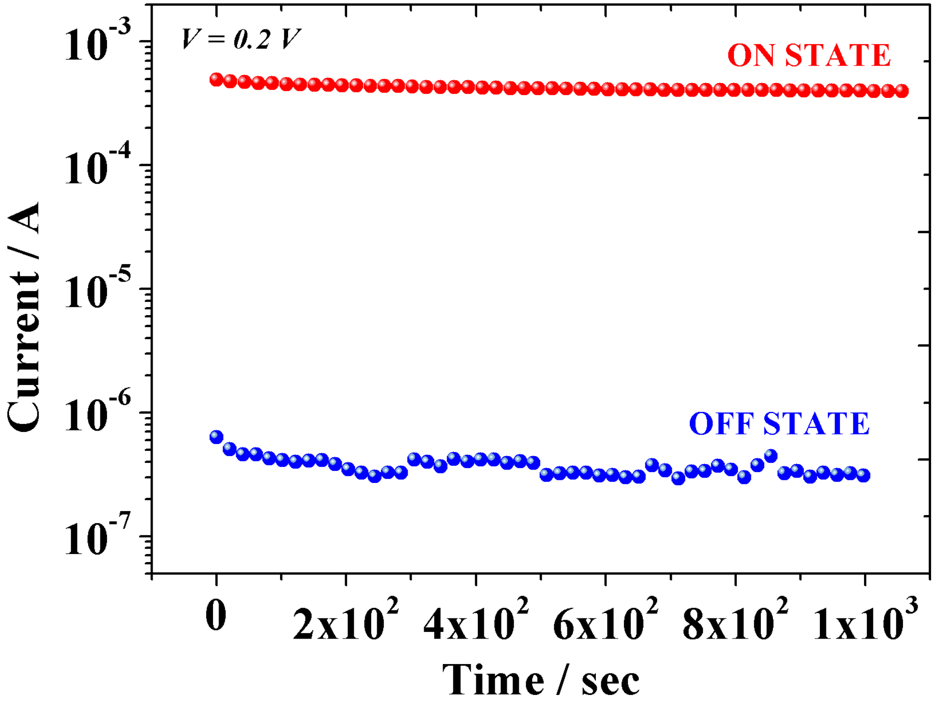
ITO/N1400(120 nm)/Au NPs/N1400(120 nm)/Ag

Parameter	Average ± error
V_{WRITE} [V]	-1.4± 0.4
V_{ERASE} [V]	+5 ± 1
I_{ON}/I_{OFF}	$(3 \pm 1)\cdot 10^4$

Electrical characterization in air

Gold Nanoparticles

GLASS/ITO/N1400(120 nm)/Au NPs/N1400(120 nm)/Ag



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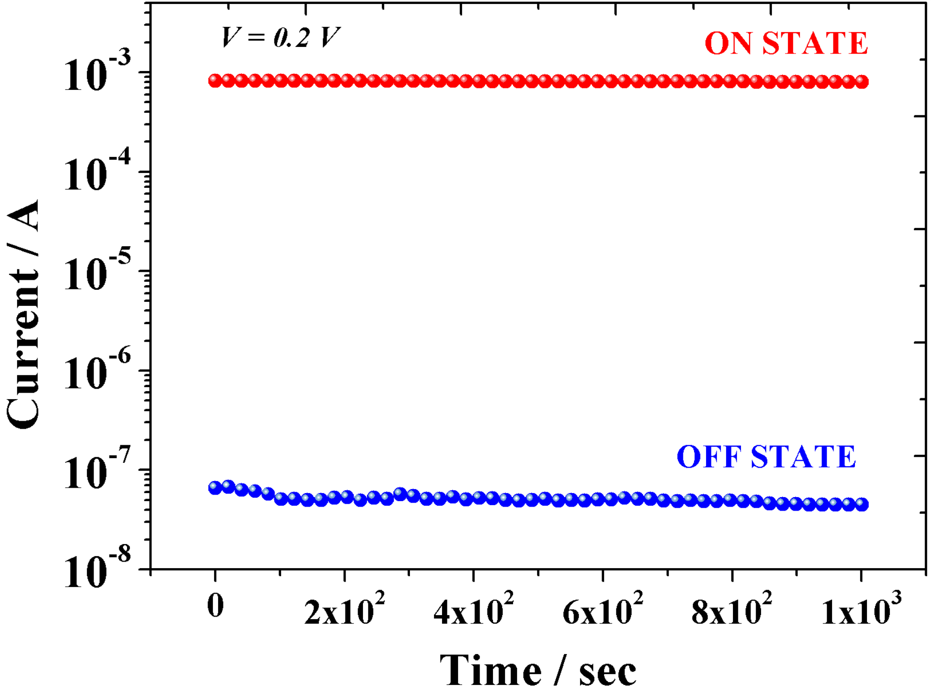

Parameter	Average ± error
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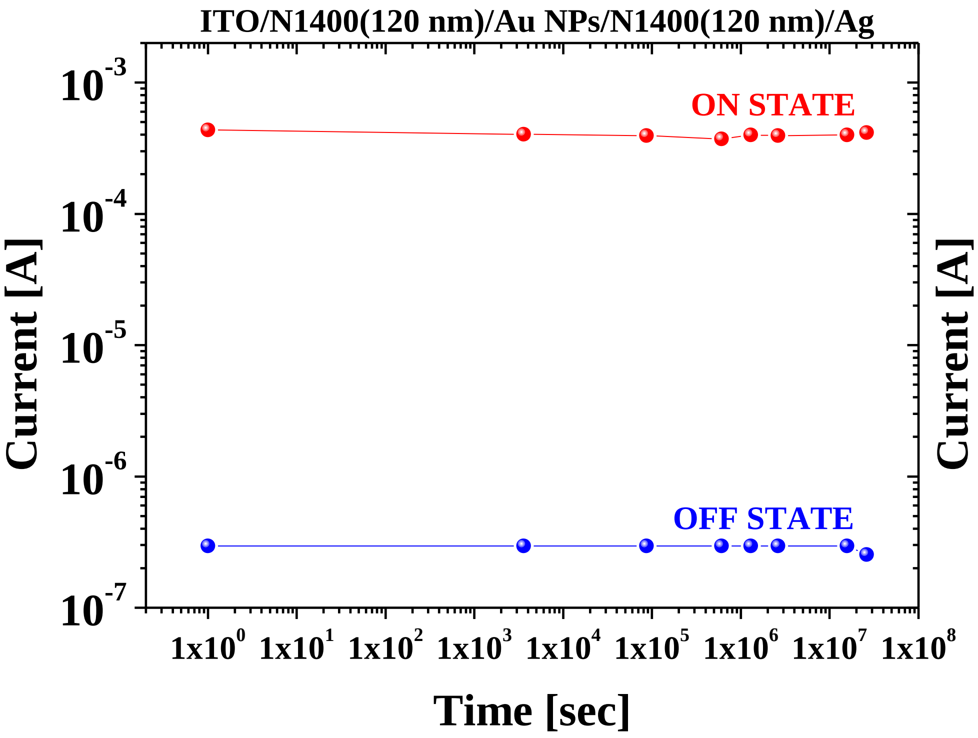
I_{ON}/I_{OFF}	$(3 \pm 1)\cdot 10^4$

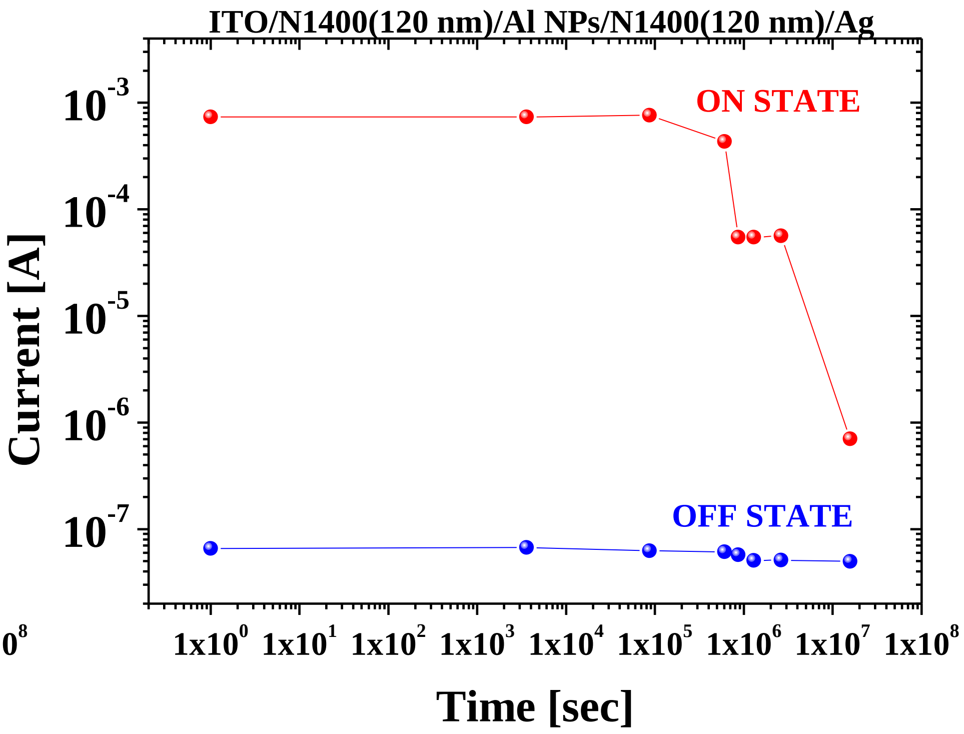
Electrical characterization in air: retention time tests

Gold Nanoparticles



- **Retention time ~ $6.3 \cdot 10^7$ sec (24 MONTHS)**

Aluminum Nanoparticles



- **Retention time < $1.7 \cdot 10^5$ sec (6 Months)**

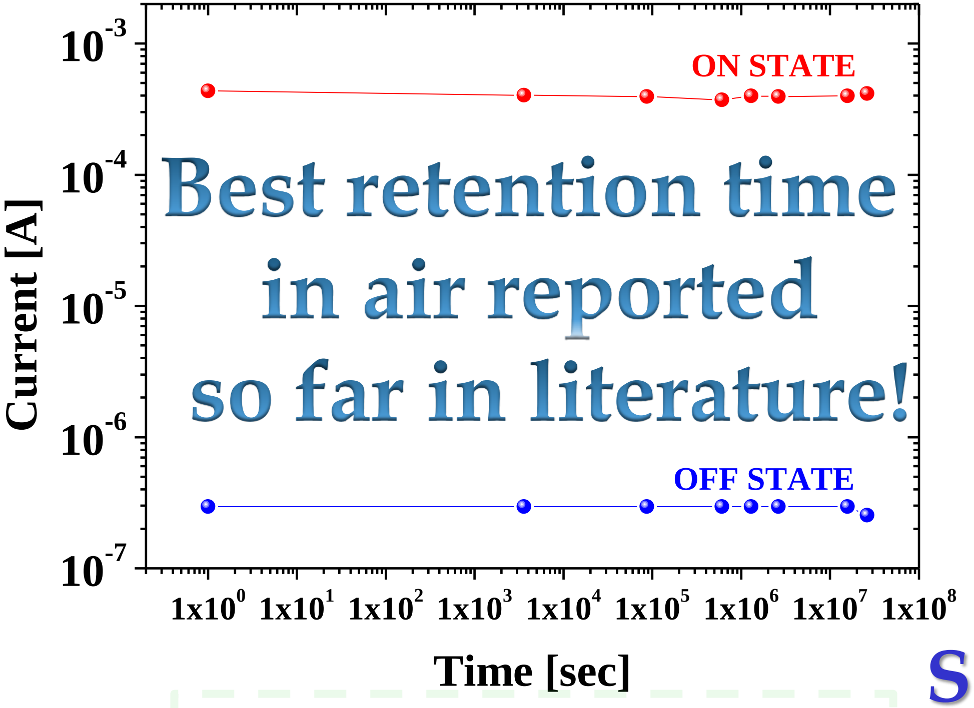
G. Casula et al., *Organic Electronics* 18, 17-23 (2015)

Electrical characterization in air: retention time tests

Gold Nanoparticles

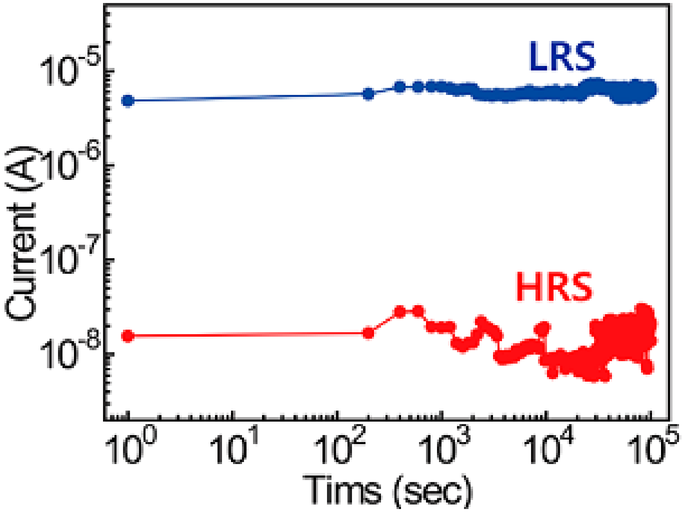
Aluminum Nanoparticles

ITO/N1400(120 nm)/Au NPs/N1400(120 nm)/Ag



Best retention time in air reported so far in literature!

- **Retention time ~ 6.3 · 10^7 sec (24 <u>MONTHS</u>)**



Hwang et al., Nano Lett.2012, 12, 2217−222

- Retention time < 1.7 · 10^5 sec (6 Months)

So far…Maximum retention time <u>in air</u> in the order of few days

G. Casula et al., *Organic Electronics* 18, 17-23 (2015)

Morphological characterization

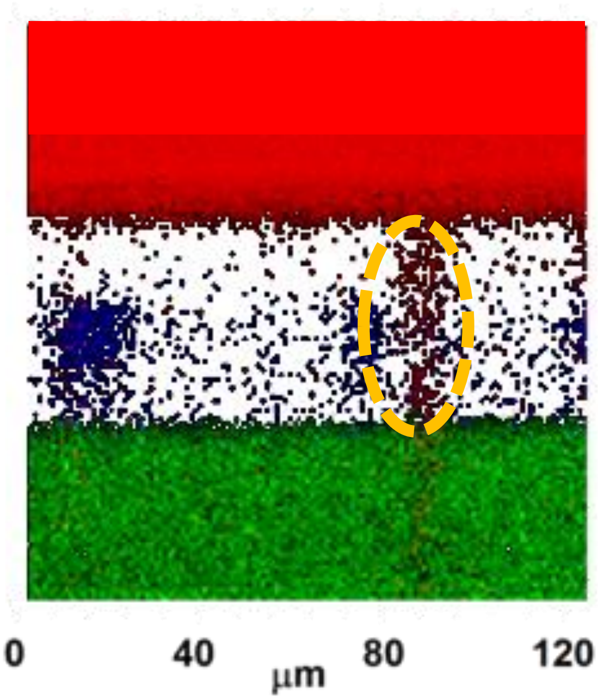
Time of Flight Secondary Ion Mass Spectrometry

🟥 Ag

🟩 ITO

⬜ N1400

🟦 NPs

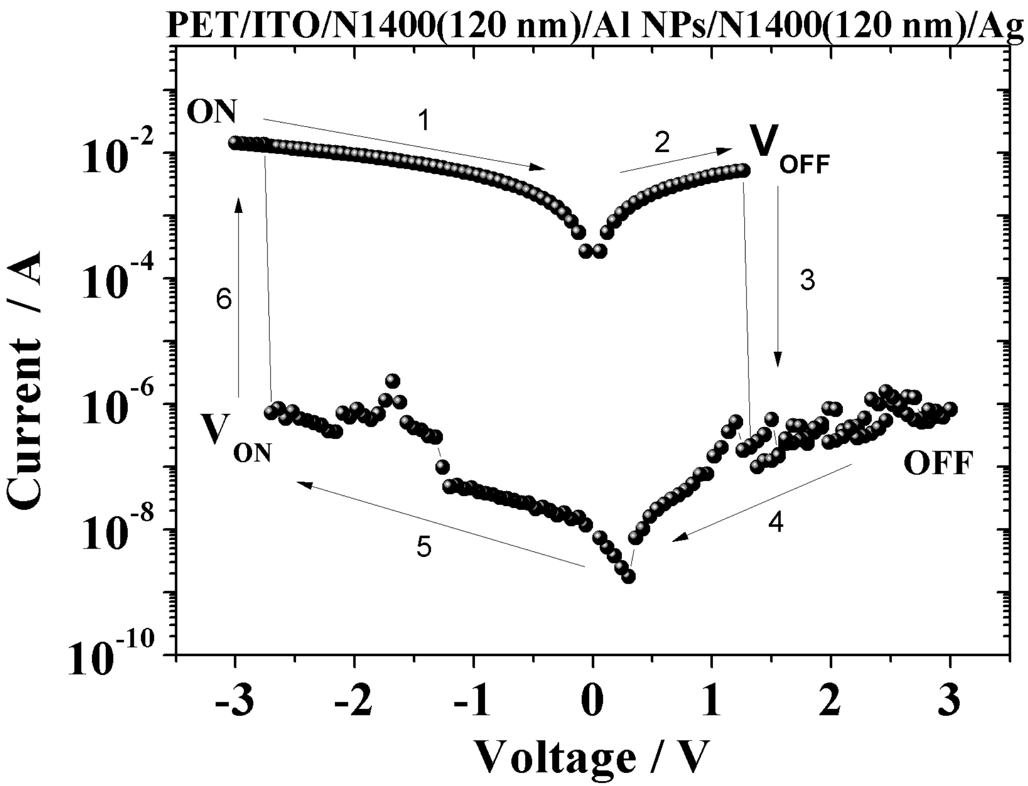


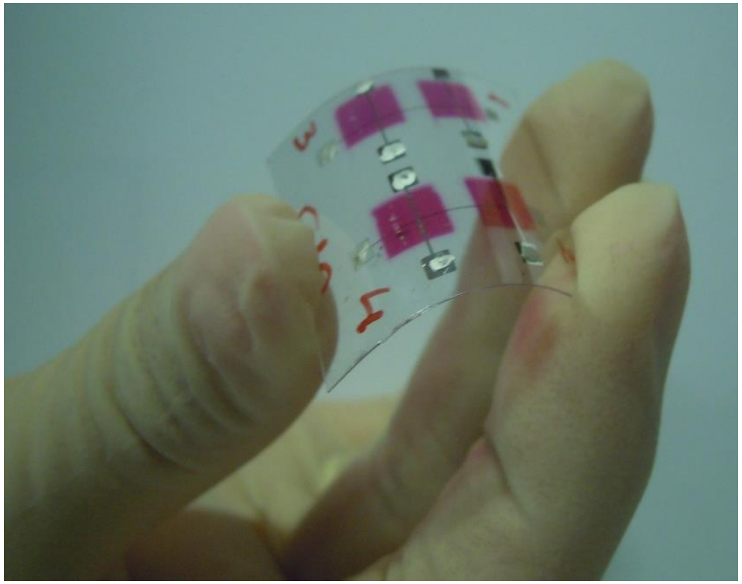
Filamentary conduction

Two dimensional (XZ) cross sections extrapolated from the 3D ToF-SIMS images of a written memory element.

G. Casula et al., *Organic Electronics* **18**, 17-23 (**2015**)

A step forward: flexible substrates

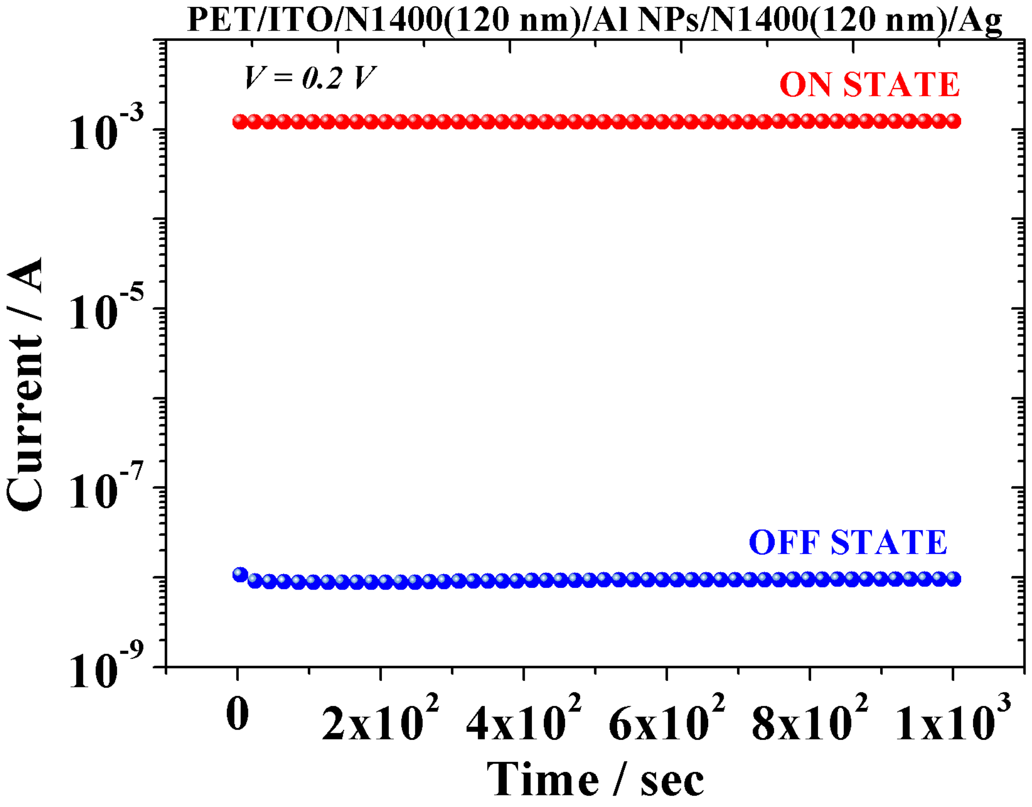


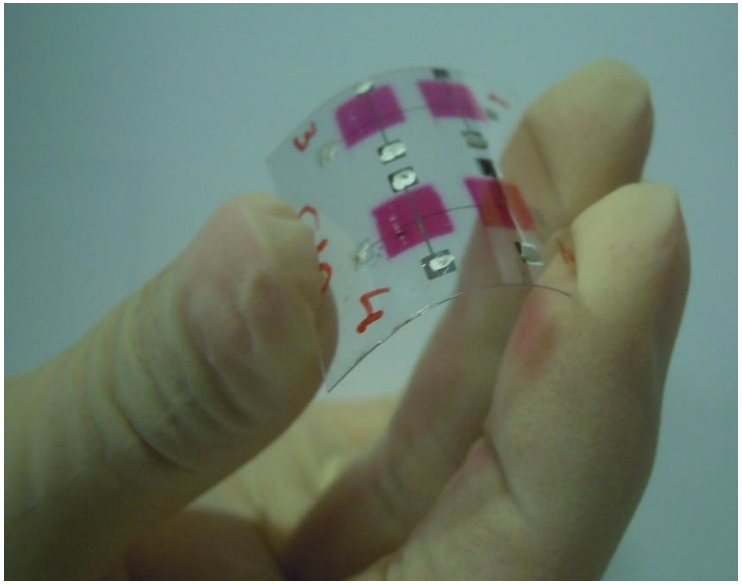


Parameter	Average ± error
V_{WRITE} [V]	-2.2± 0.5
V_{ERASE} [V]	+2.2 ± 0.6
I_{ON}/I_{OFF}	(2 ± 1)·10^5

87% of devices showed a reproducible switching behavior

A step forward: flexible substrates





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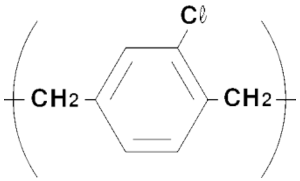
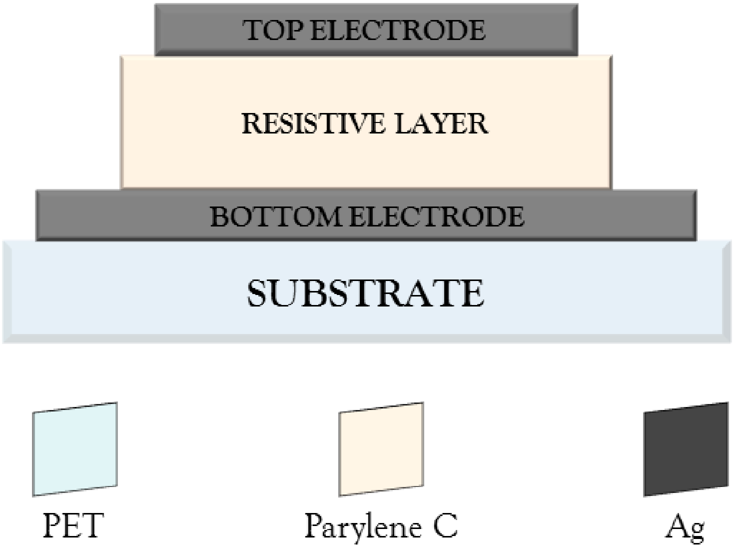
I_{ON}/I_{OFF}	$(2 \pm 1)\cdot 10^5$

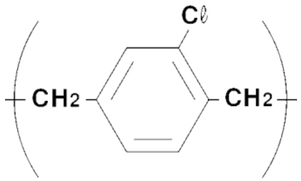
G. Casula et al., *Advanced Electronic Materials* 1(12), (2015)

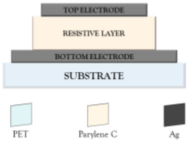
Parylene C based memories





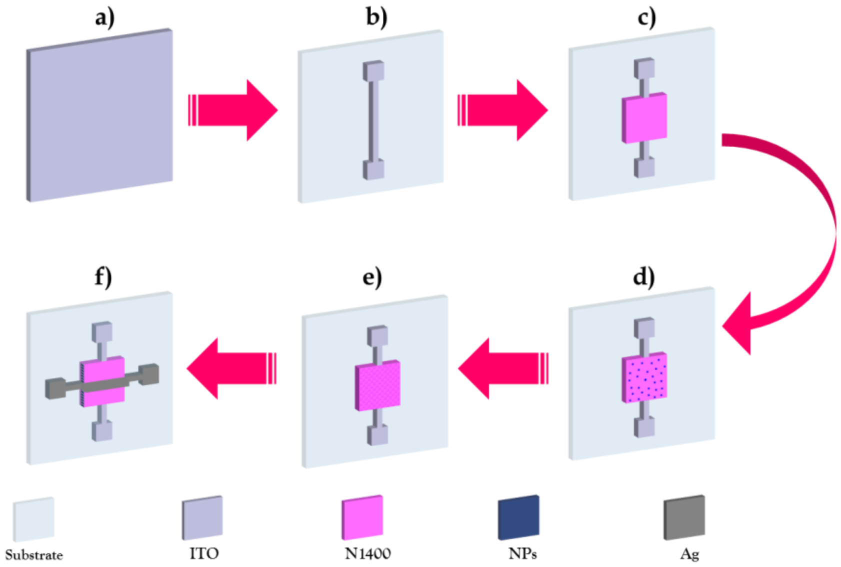
Parylene C based memories



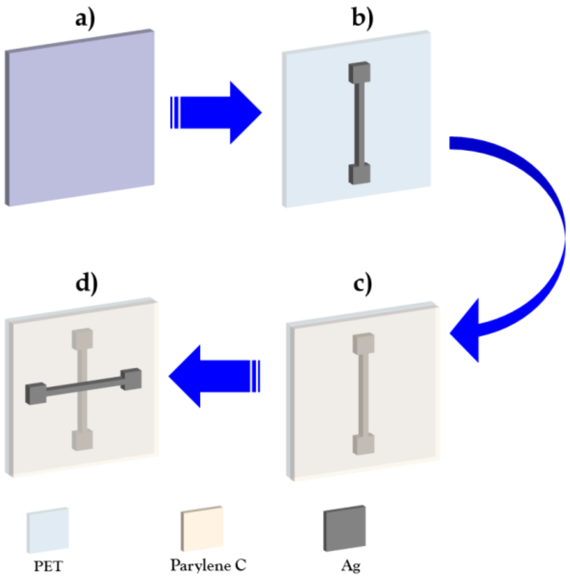


What's better??

N1400 based memories



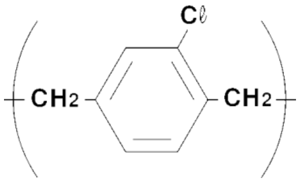
Parylene C based memories

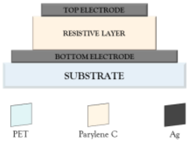


- Resistive layer deposition requires three thermal evaporations

- Faster: resistive layer in one step!
- Easier
- Larger throughput

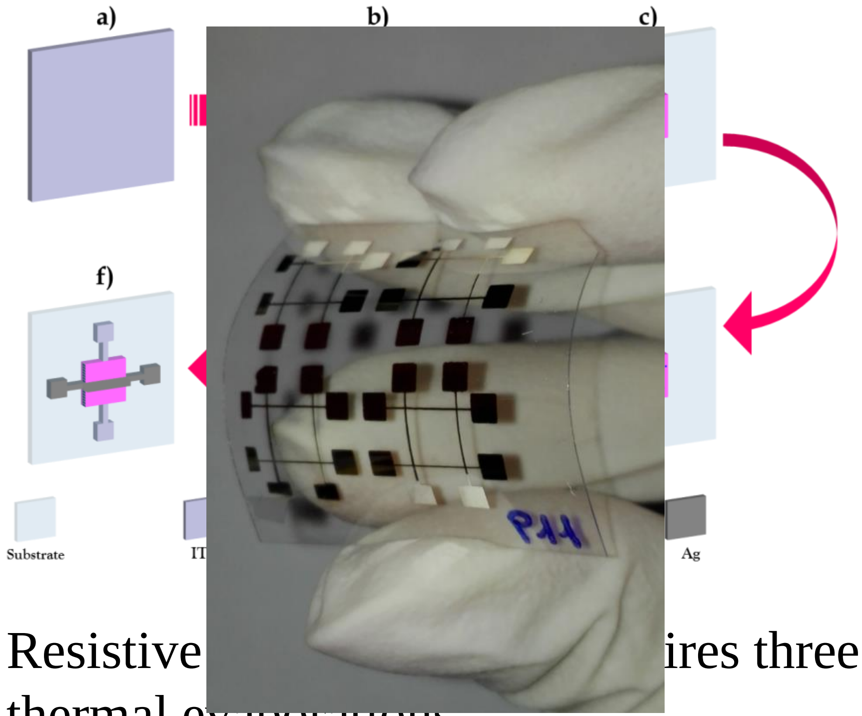
Parylene C based memories





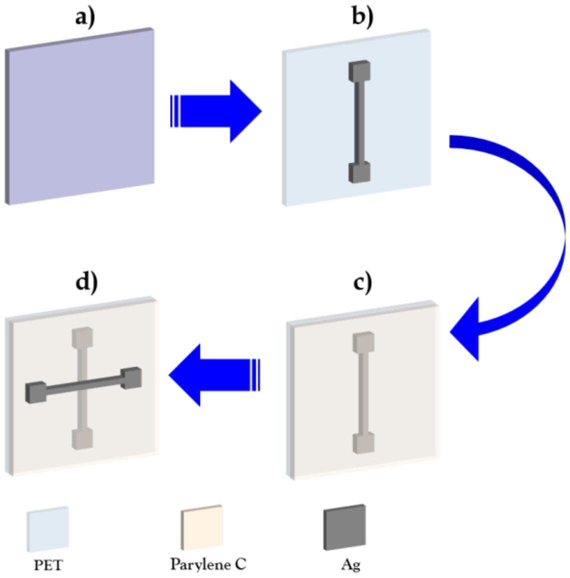
What's better??

N1400 based memories



- Resistive ires three thermal evaporations

Parylene C based memories



- Faster: resistive layer in one step!
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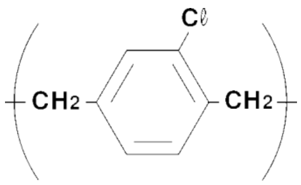
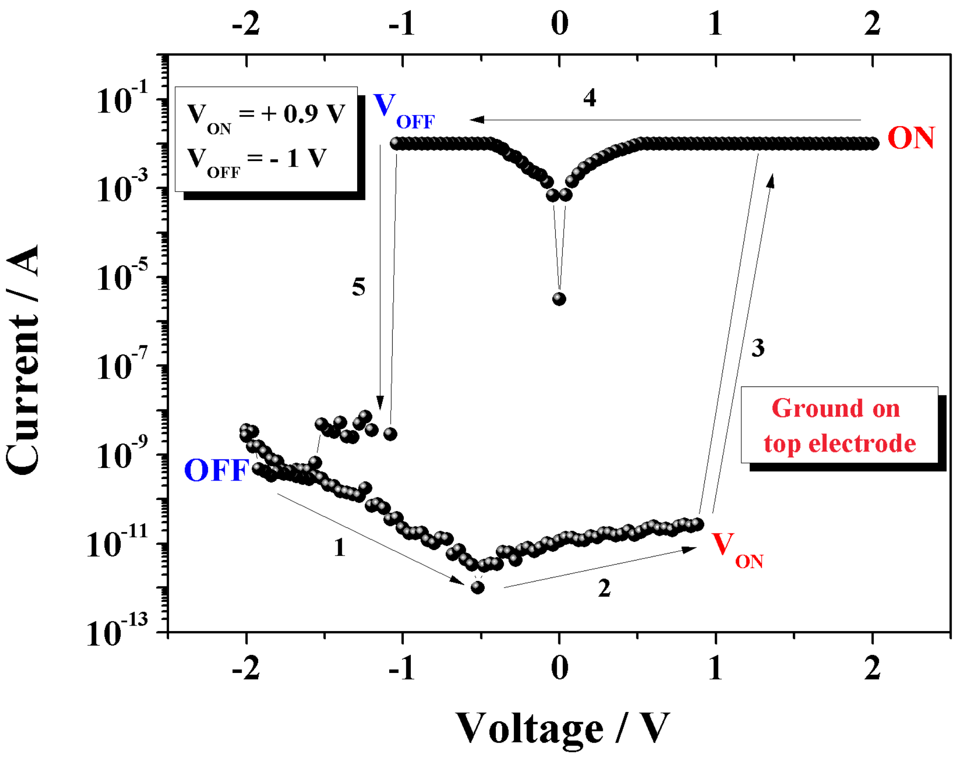
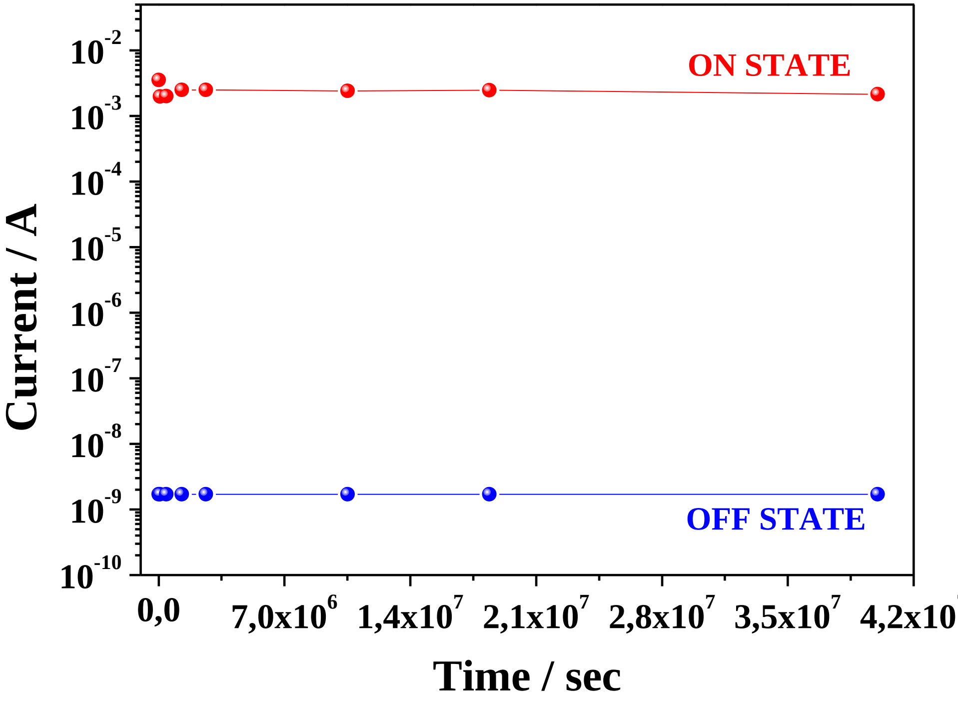
Parylene C based memories



Electrical characterization in air





Parameter	Average ± error
V_{ON} [V]	+0.7± 0.05
V_{OFF} [V]	-0.61 ± 0.02
I_{ON}/I_{OFF}	$(2.7\pm 0.3)\cdot 10^8$

Retention time so far ~ 15 MONTHS