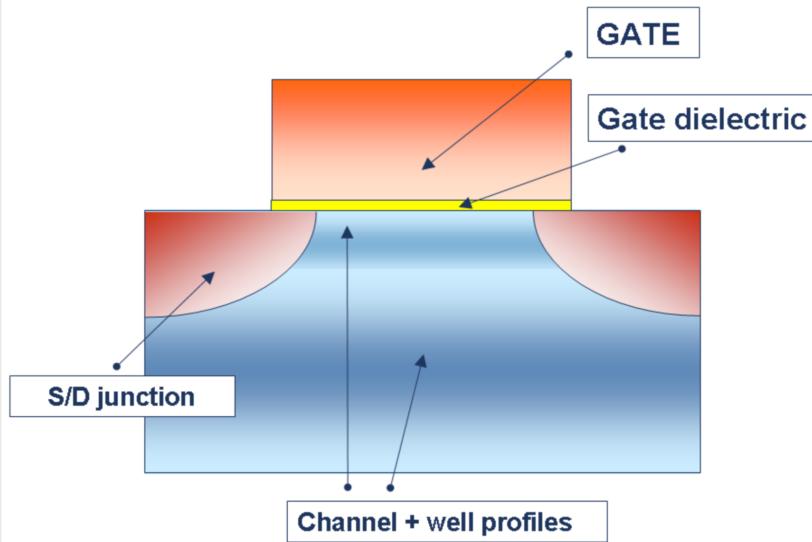
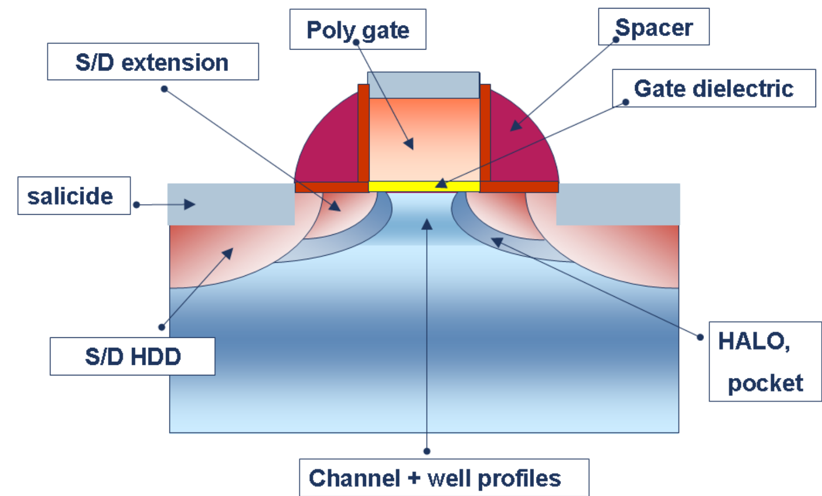
DSM MOS layout

‘classical=texbook’ MOSFET structure

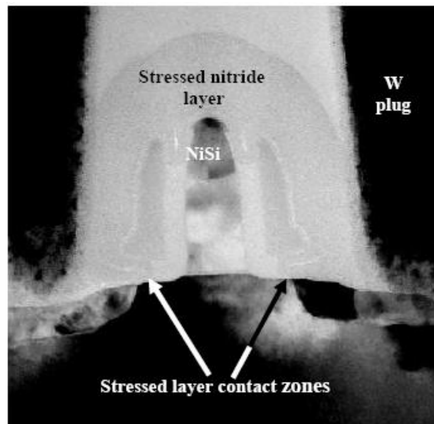


typical ‘advanced’ MOSFET Structure

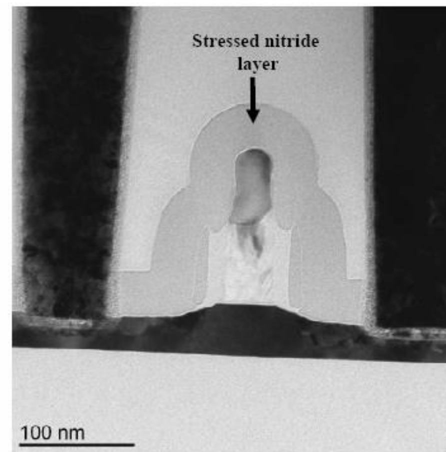


DSM MOS layout

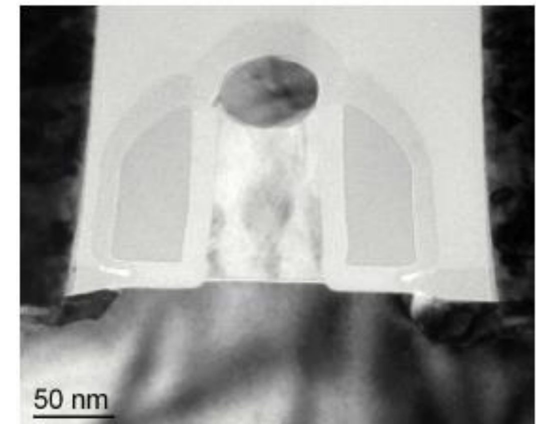
Different foundry = different device process!



Intel



IBM



TSMC

CMOS process flow :

front end (FE) and back end (BE)

DSM MOS process

Two different process flows are required:

- front end of line (FEOL) process flow
- back end of line (BEOL) process flow

FEOL the transistors are fabricated on the substrate

BEOL all the contacts and metallizations are generated

DSM MOS process

Advanced CMOS process flow

Active area definition
Well & channel doping
Gate electrode
S/D HALO / extensions
Spacers
HDD junctions
Silicides

← **CMOS Front End of Line process**

PMD
Contact
Metal1
IMD1
Via1
Metal2
....

← **CMOS Back End of Line process**

Techniques: oxidation

Oxidation is the process by which a layer of silicon dioxide is grown on the surface of a silicon wafer.

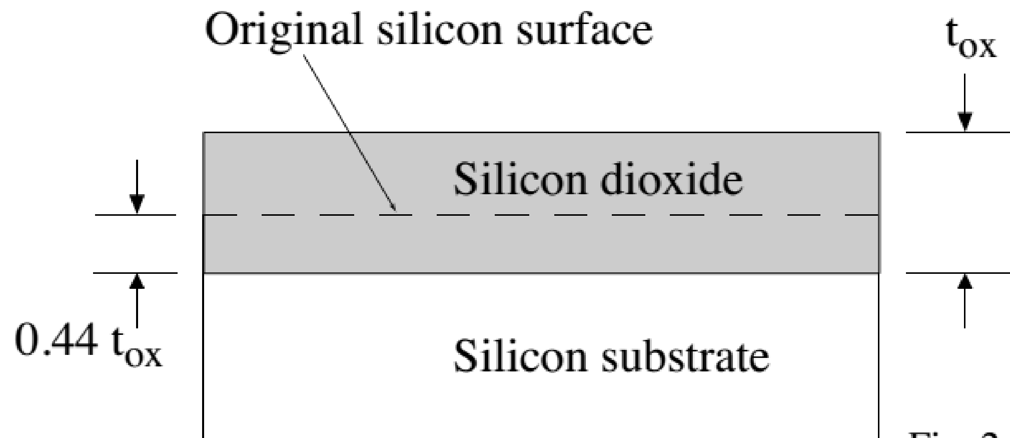


Fig. 2.1-2

Uses:

- Protect the underlying material from contamination
- Provide isolation between two layers.

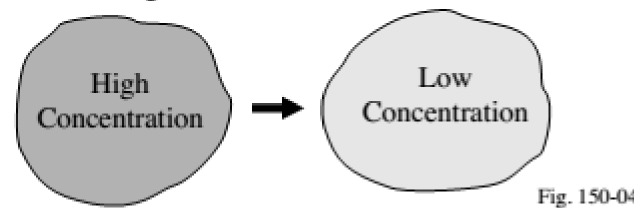
Very **thin oxides** (100Å to 1000Å) are grown using **dry oxidation** techniques.

Thicker oxides (>1000Å) are grown using **wet oxidation** techniques.

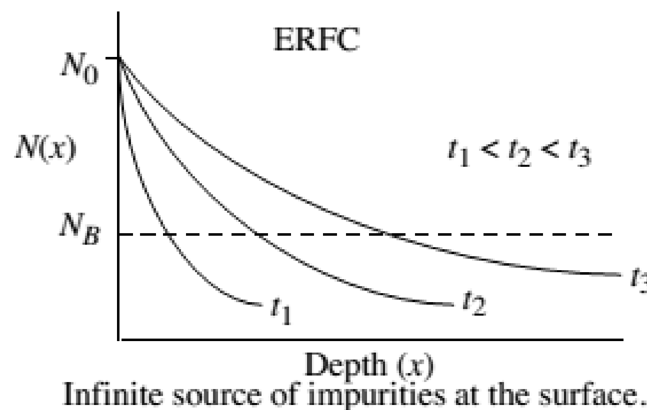
Techniques: diffusion

Diffusion is the **movement of impurity atoms** at the surface of the silicon into the bulk of the silicon.

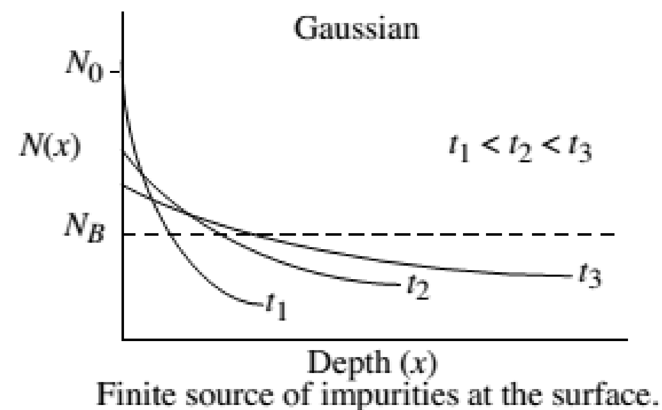
Always in the direction **from higher concentration to lower concentration.**



Diffusion is typically done at high temperatures: 800 to 1400°C



Infinite source of impurities at the surface.



Finite source of impurities at the surface.

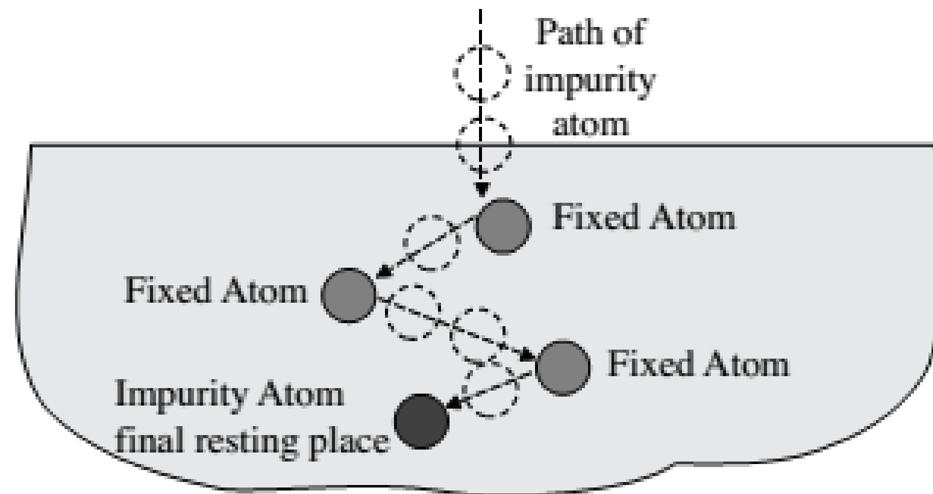
Fig. 150-05

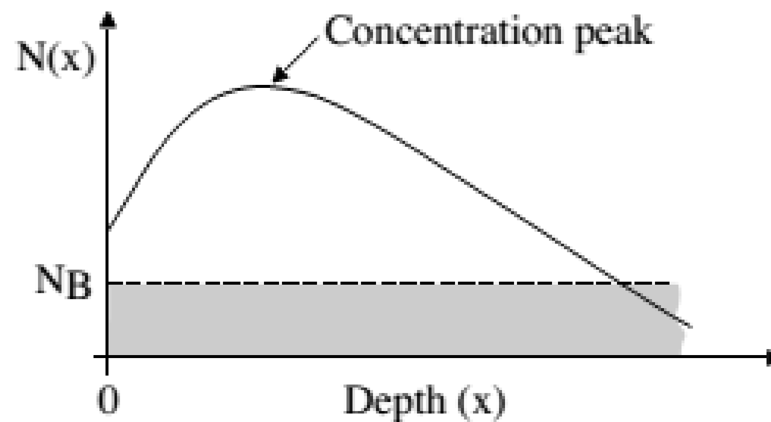
Techniques: ion implantation

Ion implantation is the process by which **impurity ions are accelerated** to a high velocity and physically lodged into the target material.

- **Annealing is required** to activate the impurity atoms and repair the physical damage to the crystal lattice. This step is done at 500 to 800°C.
- Ion implantation is a **lower temperature** process compared to diffusion.
- **Can implant through surface layers**, thus it is useful for field-threshold adjustment.
- **Can achieve unique doping profile** such as buried concentration peak.

Techniques: ion implantation





Techniques: depositions

Deposition is the means by which various materials are deposited on the silicon wafer.

- Silicon nitride (Si_3N_4)
- Silicon dioxide (SiO_2)
- Aluminum
- Polysilicon

There are various ways to deposit a material on a substrate:

- Chemical-vapor deposition (CVD)
- Low-pressure chemical-vapor deposition (LPCVD)
- Plasma-assisted chemical-vapor deposition (PECVD)
- Sputter deposition

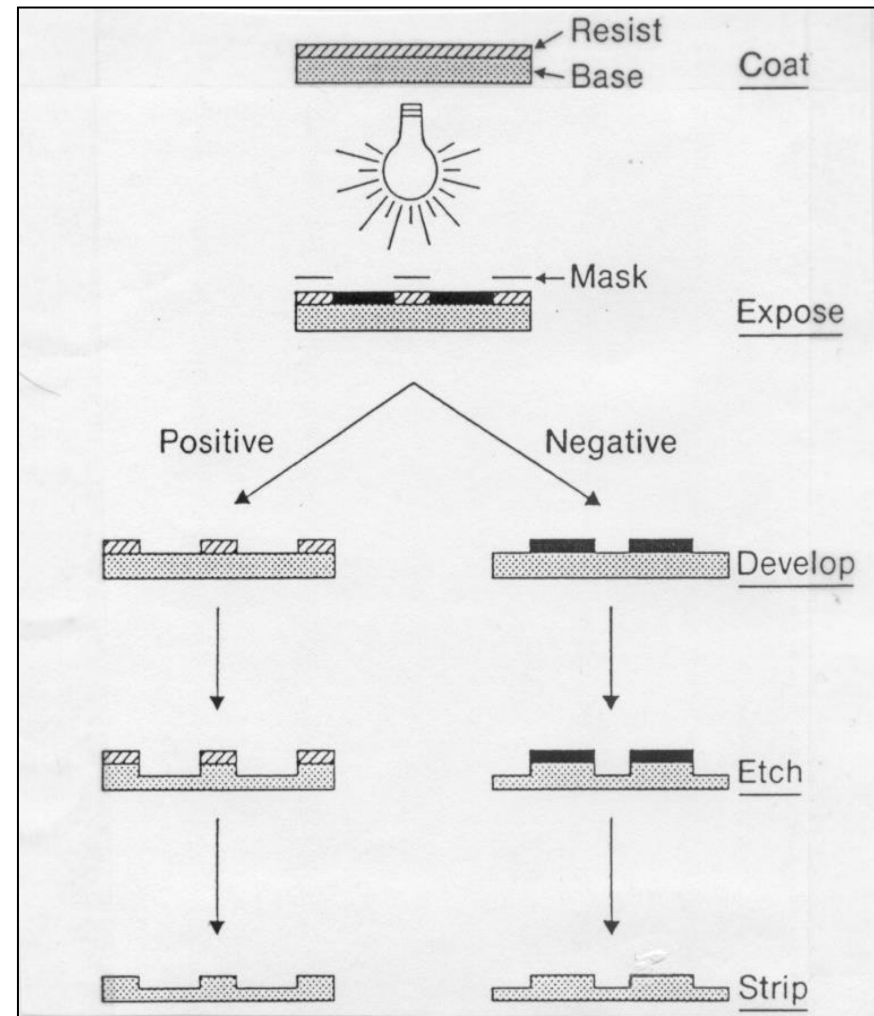
Material that is being deposited using these techniques covers the entire wafer and requires no mask.

Techniques: photolithography

CMOS processing requires only 3 'steps' !
(but repeated a lot of time…)

- deposition
- pattern definition (photo-lithography)
- remove material (etch)

$$resolution = k_1 . \frac{\lambda}{NA}$$



Techniques: etching

Purpose: remove material

Wet etch:

mostly **isotropic**, for 'large' patterns, **uncompatible with device scaling**
Chemical action, dip wafers in wet bath

Dry etch:

anisotropic trenches possible, compatible with high density,
plasma reactor, both physical and chemical etch involved

Techniques: dry etching

Dry etching techniques are used in micro-engineering to face the main drawbacks of **wet (purely chemical) etching**, which are:

- the presence of irreproducible disturbances from bubbles, flow pattern, etc.,
- handing with corrosive and toxic materials
- limitation of the minimum achievable dimension
- the impossibility to obtain vertical trenches.

Techniques: dry etching

Dry etching may be defined as the use of radical species and/or energetic ions from a cold plasma (or ion beam source) to **remove material where there is no mask material**.

The action of plasma etch is **both physical** (increased anisotropy and decreased selectivity) and **chemical** (more selective and isotropic).

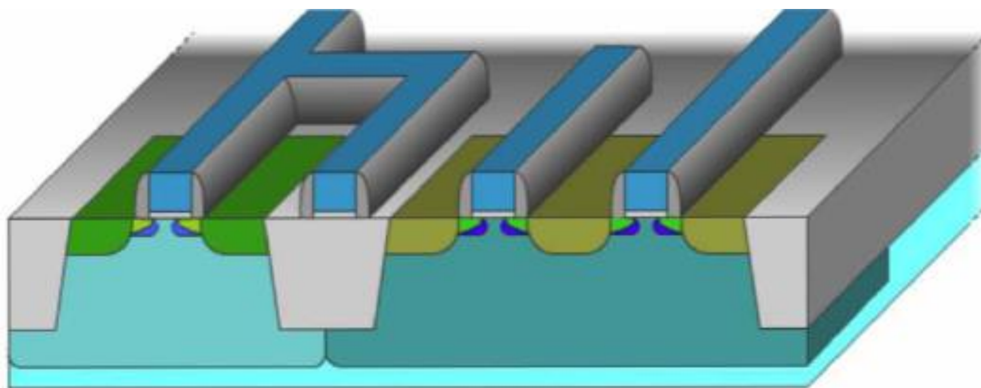
The main process variables are:

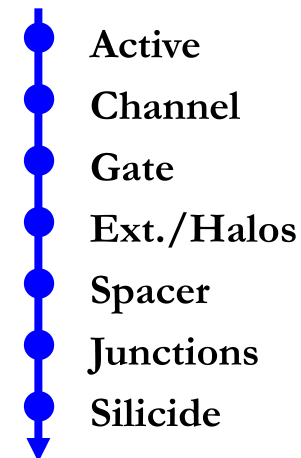
- gas mixture (affecting etch rate and profile shape),
- the flow rate (effect on etch rate through residence time),
- pressure (etch rate, profile shape, selectivity),
- RF power (etch rate through dislocation rate),
- wafer temperature (profile shape and chemistry),
- self-bias of the chuck (selectivity, etch rate and shape profile)

Front End Of Line (FEOL)

These are the 7 FEOL modules that will be introduced (and later correlated with electrical performance)

1. Active area module
2. Channel doping module
3. Gate electrode module
4. Source/drain extensions module
5. Spacer module
6. Junctions module
7. Silicide module





Front End Of Line (FEOL)

The active area module is the **first module** in the FEOL process flow.

The purpose of the active area module is twofold :

- **It defines the active regions.** These are the regions in which the (active) transistors will be realized.
- **It realizes good lateral insulation between the different active regions.** These lateral insulation areas are called the **field regions or field oxides, FOX** (SiO2 dioxide, the oxide of silicon).

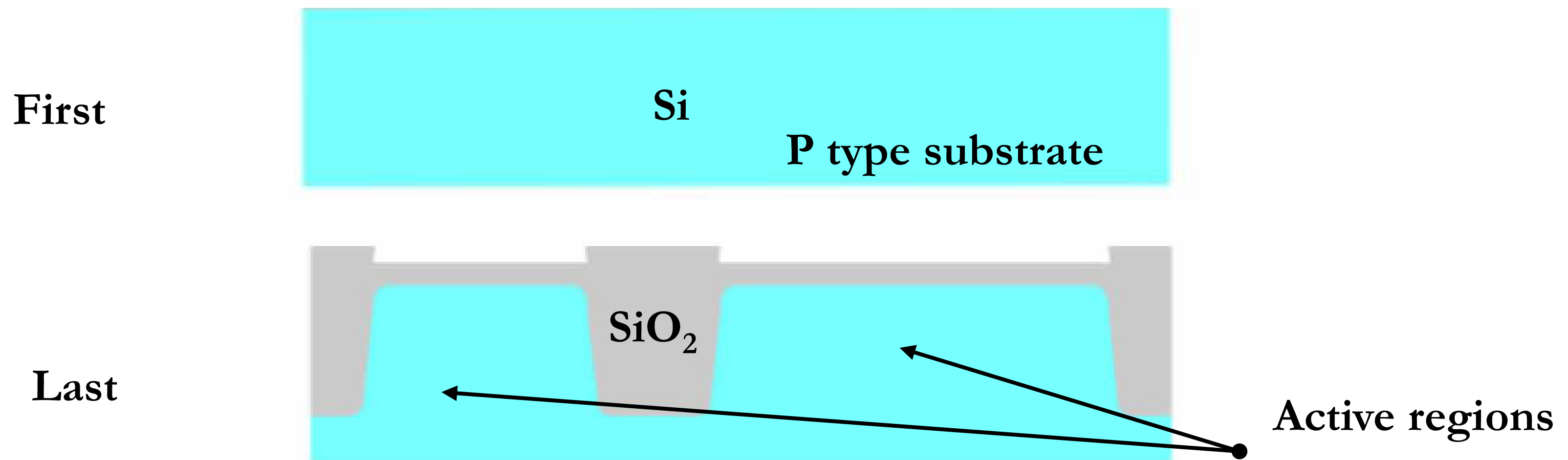
THEY ARE NECESSARY TO INSULATE TRANSISTORS FROM EACH OTHER.

Shallow trench isolation

Purpose:

- Define Active regions where transistors are located.
- Good isolation between transistors & parasitic transistors formed by interconnecting poly-Si/metal stripes.

It all starts from a p type doped silicon wafer



Shallow trench isolation

Pad Oxide Growth

It all starts with the silicon wafer on which **a thin (15-20 nm) oxide is thermally grown**. This oxide layer is called the pad oxide and is a **buffer material.**

Depositing the **silicon nitride (hard material) immediately** on the silicon wafer **would cause internal stress, damaging the wafer.** Hence the purpose of **pad oxide is to absorb most of the stress.**

Afterwards a protective silicon nitride (SiN) layer is deposited on the wafer using a technique called "LPCVD" (LOW Pressure Chemical Vapour Deposition).

Silicon nitride is a strong and very hard ceramic.

Shallow trench isolation

To create the trenches, the position where they will be located has to be defined

This is done using a **photolithography step.**

After the litho step, photo resist remains on top of the future active areas; these are the regions where the nitride should remain after the next step

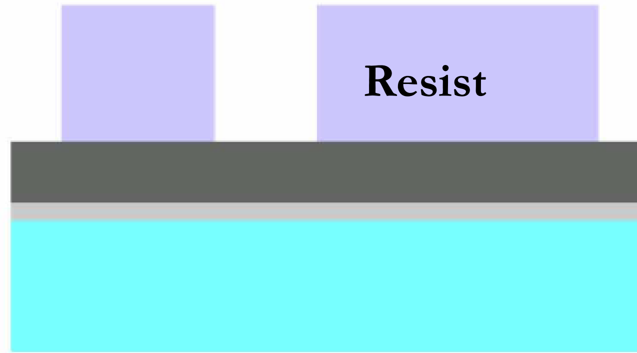
Therefore this step is called the active area litho step.

The dry etch step

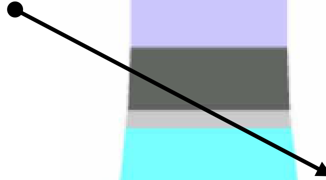
- first removes the unprotected - there is no photo resist on it – nitride above the field regions
- Afterwards the pad oxide is etched
- Finally, it etches into the silicon wafer to form trenches

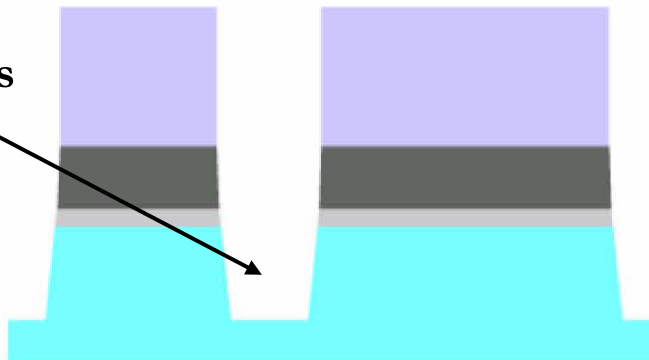
Shallow trench isolation

Pad oxide growth + nitride deposition

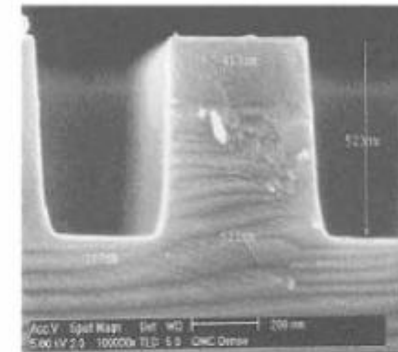


Active area lithography step





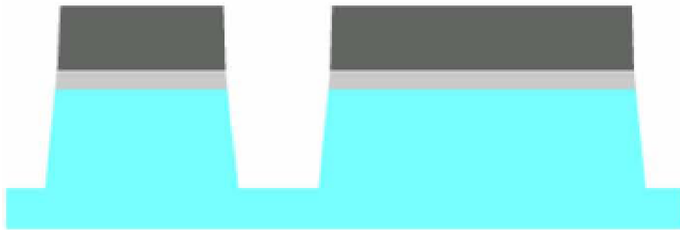
Etch



Shallow trench isolation

The resist is then removed. Depending on the fab, this can be done using various etch techniques: dry etch and wet etch or even a combination.

1) Resist removal



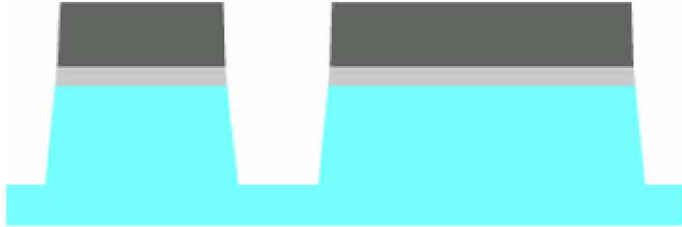
Re-Oxidation and Corner Rounding steps:

Rounded corners: HF (hydrofluoric acid) is a strong acid. A short dip in it followed by a **re-oxidation will remove the sharp corners.**

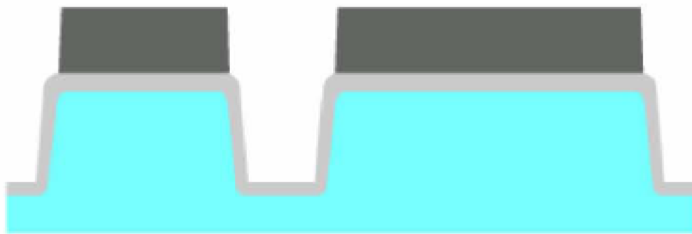
Damage repair: The silicon in the trenches is damaged by the dry-etch, causing imperfections in the lattice. **To get rid of the imperfections, the silicon is converted into oxide during the re-oxidation**.

Shallow trench isolation

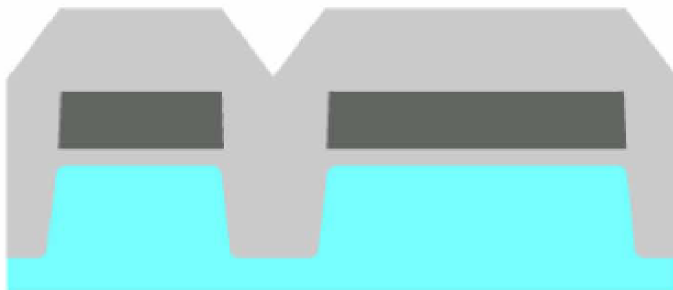
1) Resist removal



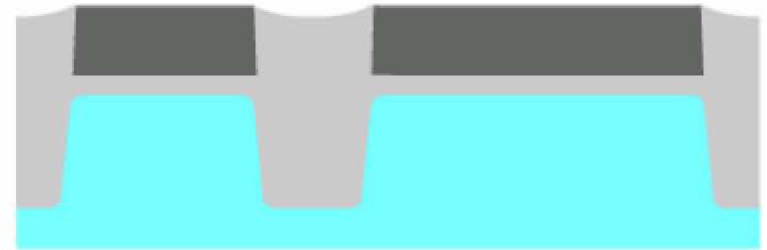
2) Sidewall oxidation, corner rounding



3) Deposition of trench filling oxide (HDP CVD)

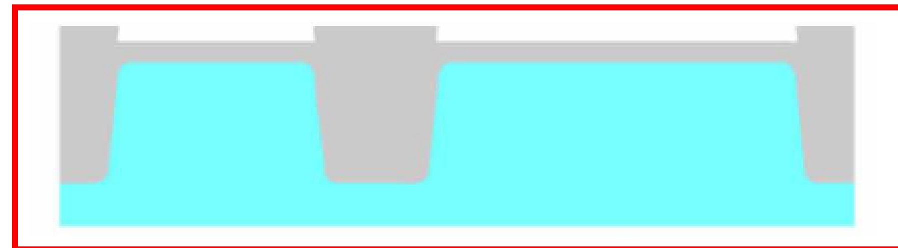


4) Oxide CMP polish step with stop on nitride



5) Field oxide recess

Removal of nitride layer



Channel doping module

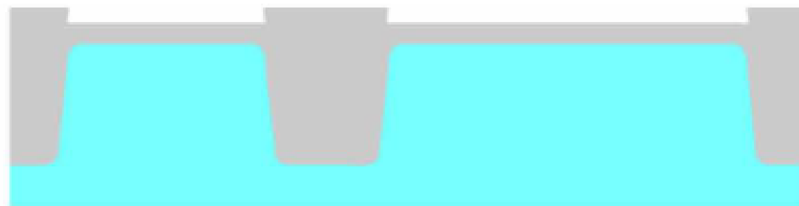
Purpose:

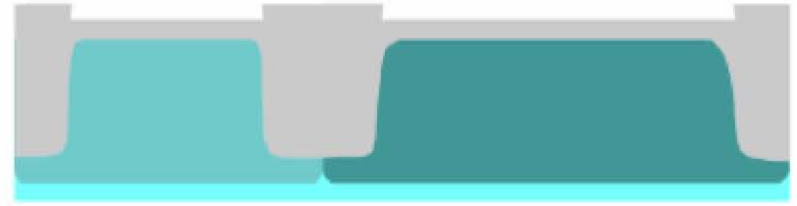
High Energy Implant

- Define P- & N-type regions for NMOS and PMOS
- Set high doping concentration underneath the field-oxide

Low Energy Implant

- threshold voltage adjustment
- leakage current suppression
- drive current optimization
- junction capacitance





Channel doping module

First Litho step

First Implants (n-type)

With the photo resist in place, **two successive n-type (phosphorous) implants are done.**

The first one is a *high-energy implant*.

These dopants have a high-energy and therefore they **can penetrate quite deep** into the silicon material.

- The high-energy implant results in the **bulk doping of the transistor** and in a high doping profile under the field oxides
- **Increasing the threshold voltage of the parasitic transistors.**

Channel doping module

The second one is a low-energy implant

Because of the low-energy, **the dopants will not penetrate deep into the wafer**

- The low-energy implant is required to **optimize the doping level in the channel region**, close to the surface.
- The photo resist protects the future p-regions from the n-dopants.

Channel doping module

Resist Strip

After the n-well is implemented, the photo resist is removed. Depending on the fab, **this can be done using various etch techniques**: both dry etch and wet etch or even a combination. The removal of the photo resist is called the **resist strip .**

The channel doping module is quite simple.

Second Litho step

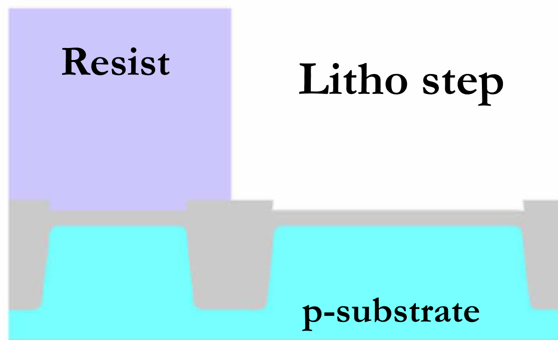
Second Implants (p-type)

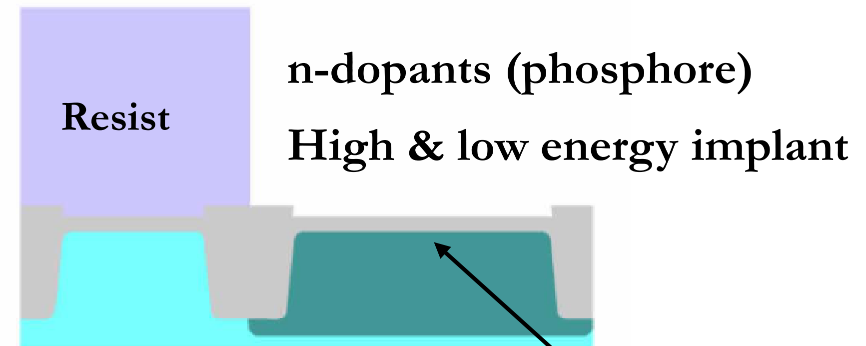
The implementation of the p-wells is **almost the same** as the implementation of the n-wells, except that this time the dopant is p-type, namely **boron (B)**

Again this is done in 2 steps: a high-energy and a low-energy implant.

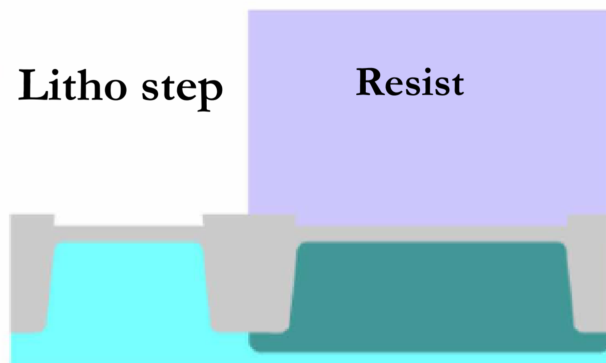
Channel doping module

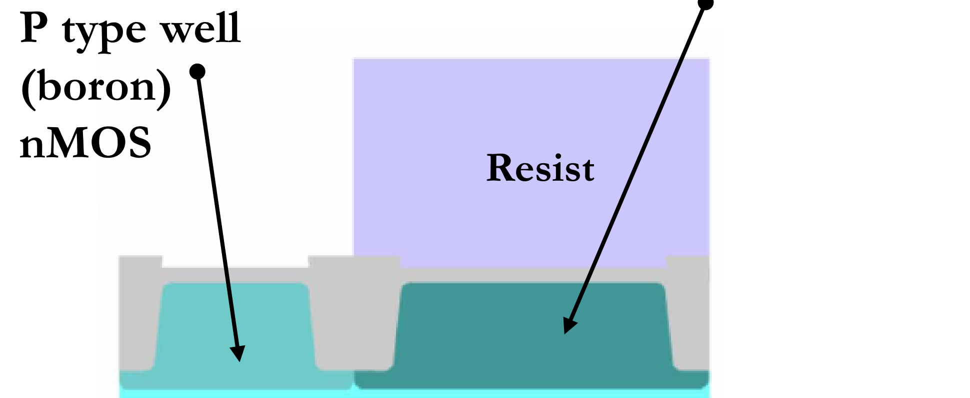
First Implants (n-type)





Second Implants (p-type)





Gate stack module: gate oxide

Purpose:

Gate oxide growth

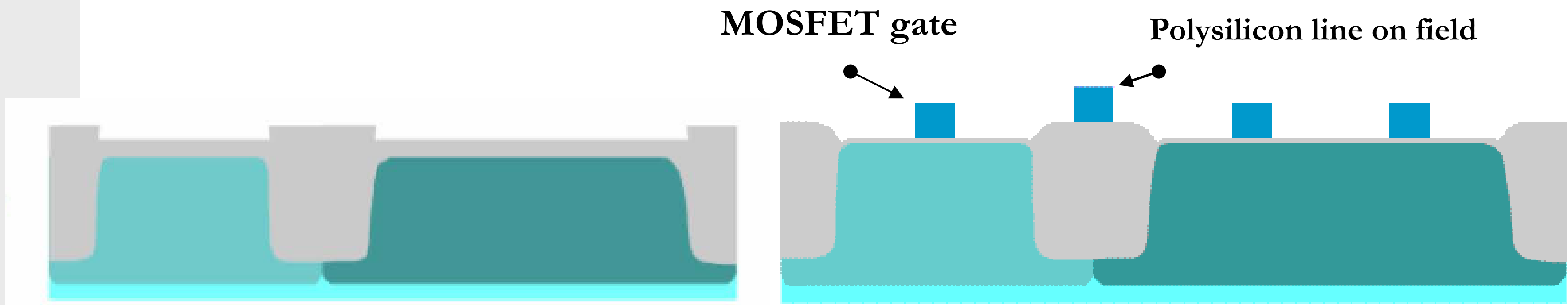
The gate oxide serves as the insulation between the gate electrode and the channel.

The gate oxide is often called gate dielectric or gate insulator.

Implementation of the gate electrodes

The gate electrode is the conductive part of the gate.

Nowadays it is **made of polysilicon** but it will be replaced by metal in future transistor generations



Gate stack module: gate oxide

In the gate electrode module a gate insulator made of oxide is grown and the gate electrode made of polysilicon is patterned.

The consecutive steps in the gate electrode module are:

- Re-oxidation
- Deposition of polysilicon
- Litho step
- Dry etch
- Resist strip

The litho step is quite critical:

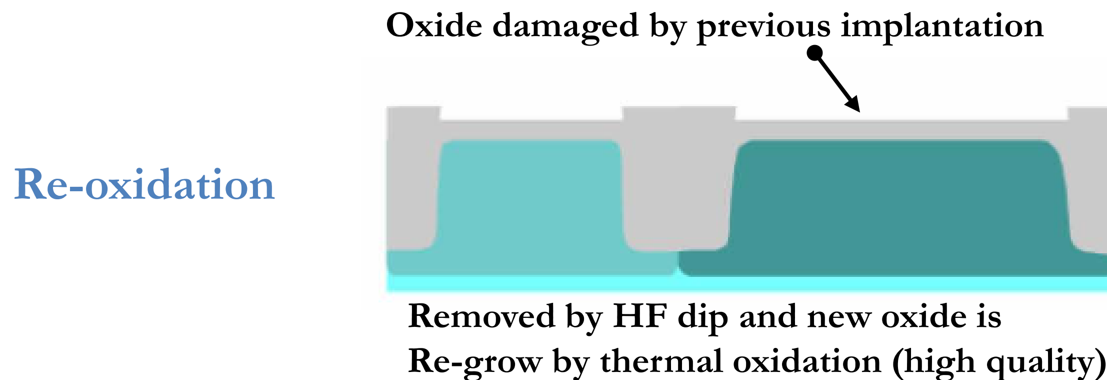
Small variation in the dimensions of the photo resist will result in transistors with different **gate length** and thus different electrical characteristics

Gate stack module: gate oxide

Re-Oxidation is the first step when processing the gate electrode.

In the previous processing module dopants were "shot" into the wafer using an ion implanter → the pad oxide is damaged

However, **the quality of the gate insulator is very important**, It has a large influence on the **threshold voltage/gate leakage** current and reliability of the transistors



The damaged pad oxide is removed doing a HF (HF = hydrofluoric acid)

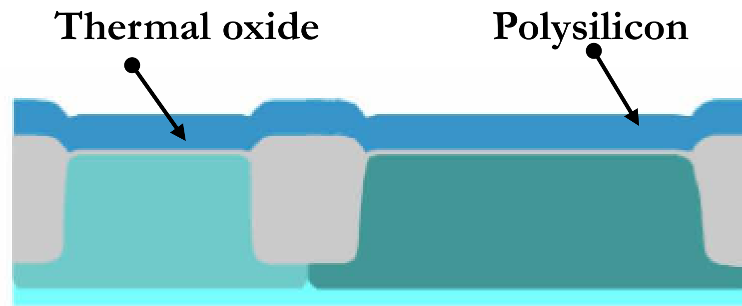
A thermal oxidation is done in order to grow an imperfection-free gate insulator.

Gate stack module: gate oxide

Deposition of Polysilicon

After the re-oxidation, **LPCVD** is used to deposit a layer of polysilicon on the wafer.

Polysilicon layer deposition

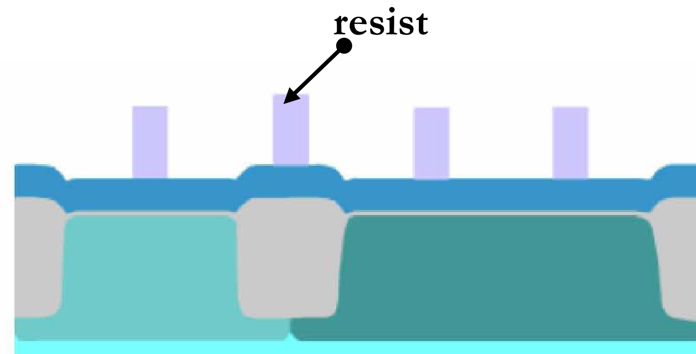


Gate stack module: gate oxide

Afterwards a **dry etch** is done, to define the electrode

(remove the polysilicon and only the polysilicon gate electrodes remain)

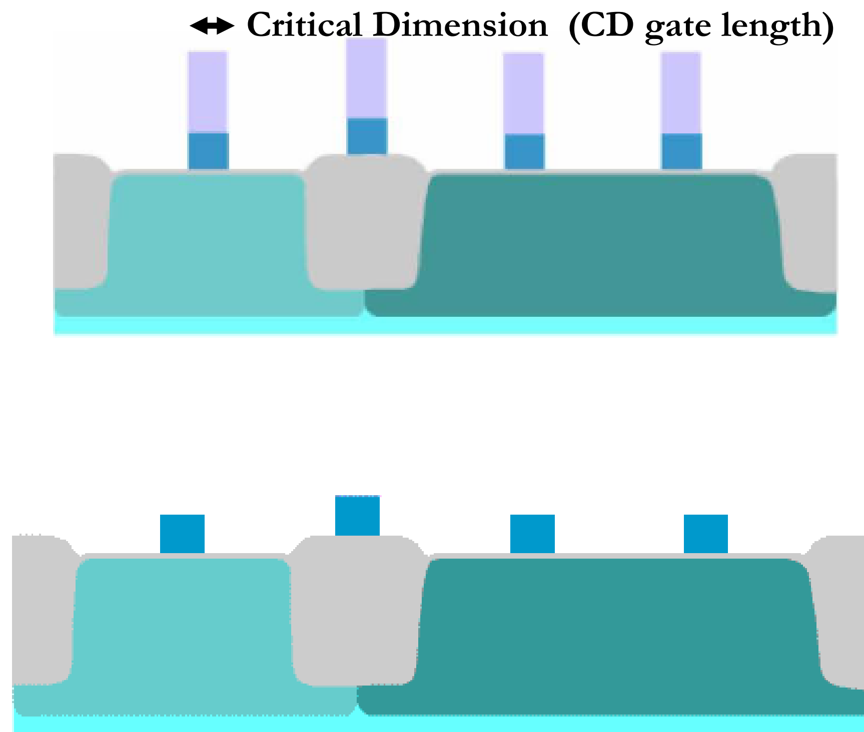
N.B. the etch chemistry used during the dry etch must have an **as high as possible selectivity towards oxide** to prevent damaging the gate insulator.



Gate stack module: gate electrode

Resist Strip

After the dry etch step, the photo resist is removed (stripped) and the gate electrode module is finished



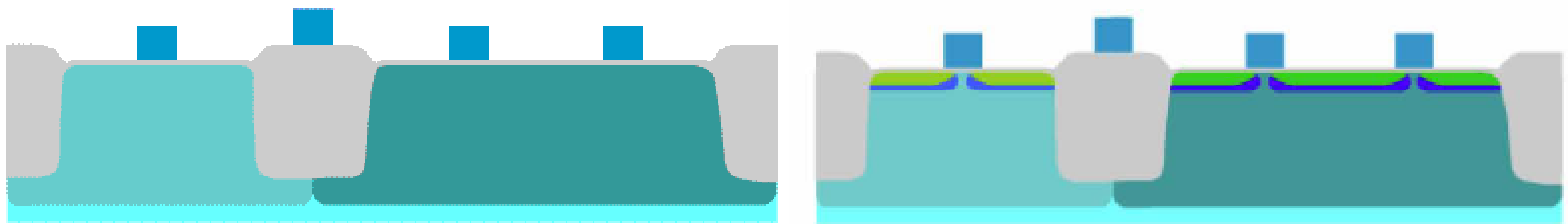
Source and drain extensions

Purpose :

- Minimize Short channel effects
- Optimize drive current/transistor performance (Rs, Rd,..)

How?

- Control maximum electrical field in the channel
- Optimize a 2-dimensional doping profile = trade off between SCE, series resistance, leakage current, drive current



Source and drain extensions

In the source/drain extensions module both source/drain extensions and **HALOs** (also called pockets) are implemented.

They are needed to suppress the physical effects, seen in the previous lectures, that start to play role when scaling down the transistor size.

Sometimes an **anti-TED (Temperature enhanced diffusion) anneal** is required in order to repair the damage caused by the previous implant.

The implant induced silicon defects (dislocations, interstitials, Vacancies..) are ideal paths for diffusion, especially during heating steps.

In recent technology research for low-temperature processes or fast anneal, in order to avoid diffusion (spike, laser,…).

Source and drain extensions

LDD implant: lightly doped extension and S/D regions

- ❑ Reduces Vt roll-off
- ❑ limit maximum electrical field (hot carrier degradations)

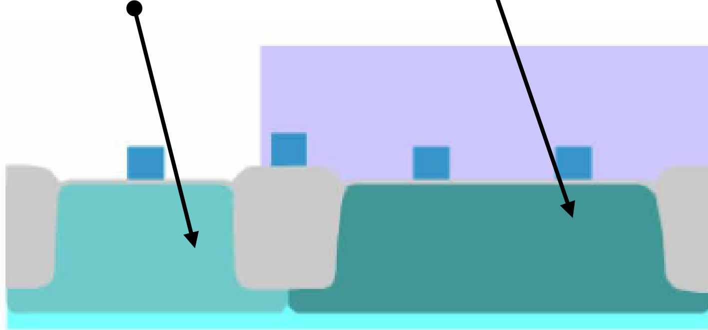
HALO or pocket implant:

- ❑ local increase of channel doping concentration around tip of LDDs.
- ❑ Suppress punch-through current
- ❑ Reduced Vth roll-off

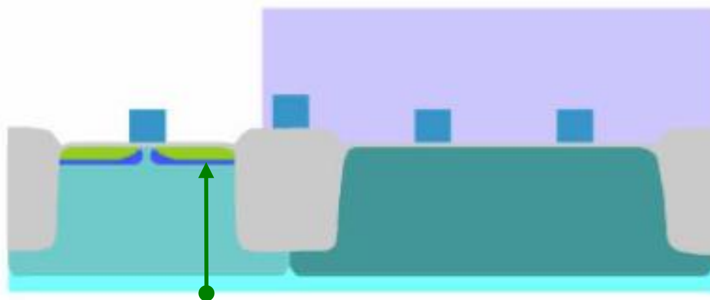
Source and drain extensions

P type well (boron)

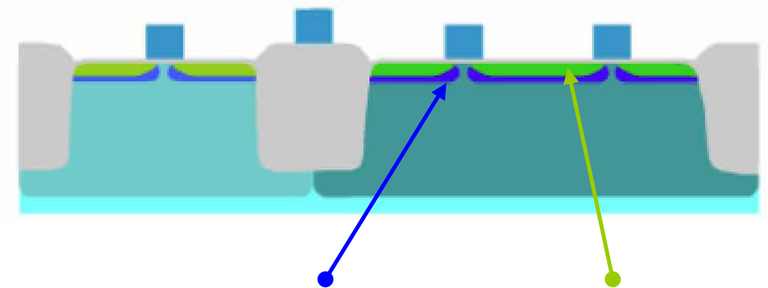
N type well (phosphore)



HALO P type implant (Boron) 23 deg < angle < 45deg)



Extension implant (Arsenic, n- type, angle~7deg)

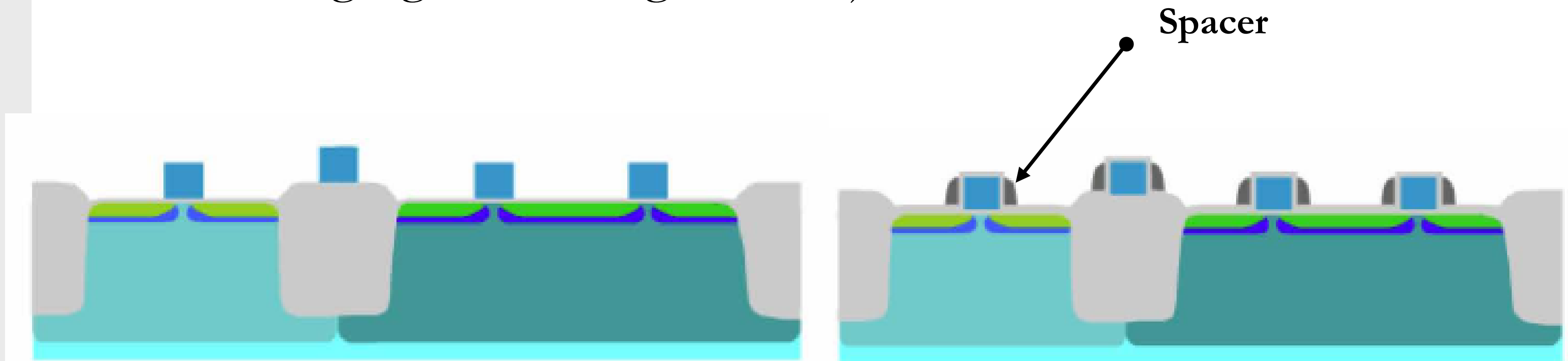


pMOS :HALO implant (Arsenic) Extention (Boron)

Space module

Purpose:

- Realize offset for highly doped junctions
- Avoid bridging between gate and junctions

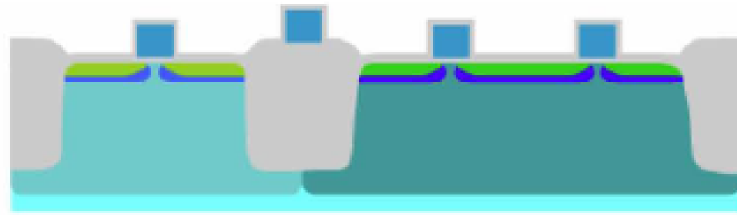


Spacers prevent dopants from diffusing under the gate during the implantation of the highly doped source/drain regions, overruling the source/drain extensions.

Spacers avoid bridging (short-circuiting) of the silicides of the gate electrodes and the source/drain regions.

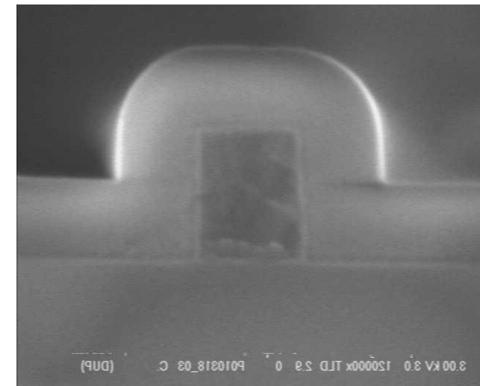
The silicides are implemented in the last module of the FEOL process flow: the silicide module

Space module

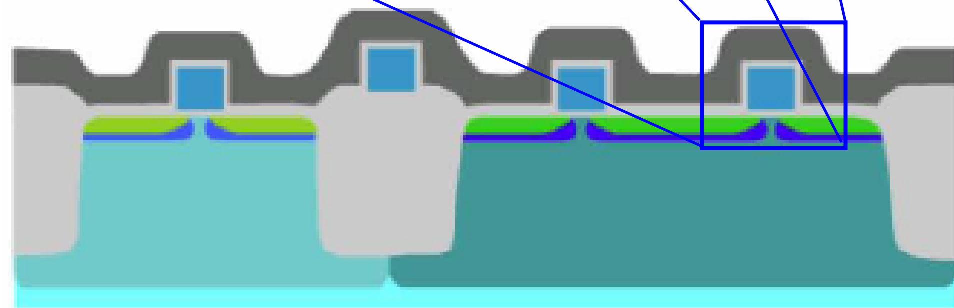


Oxide LPCV Deposition

(TEOS: stopping layer for nitride etch)

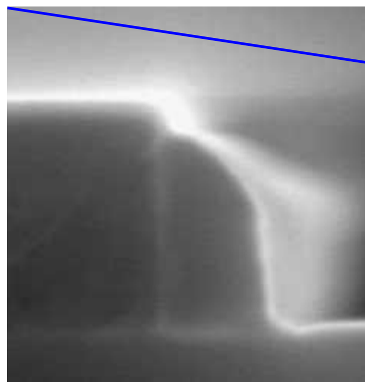


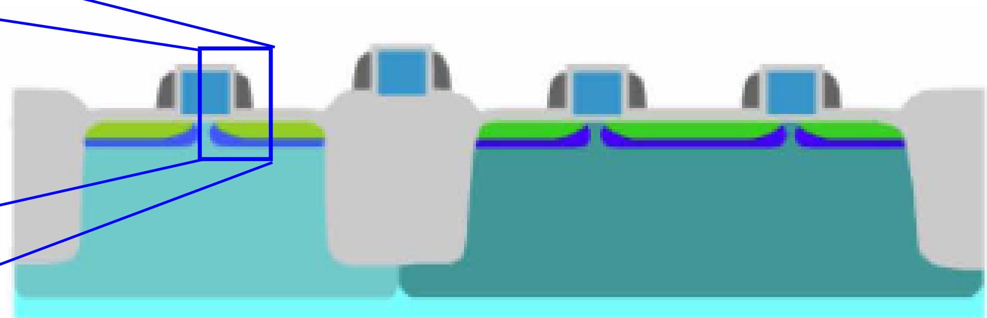
Nitride Deposition



Nitride etch

(TEOS protection and stopping layer)





Space module

LPCVD (Low Pressure Chemical Vapour Deposition) is a technique that uses a gas to deposit a layer on a surface

In this case LPCVD is used **to deposit a layer of oxide**

The **main component of the gas used is a chemical called TEOS** (Tetraethylorthosilicate), TEOS reacts with oxygen on the heated surface forming oxide.

This oxide is also needed to act as a stopping layer during dry etch later on.

Nitride Deposition

Again using LPCVD, a nitride layer is deposited. Of course this time the chemistry is different from the LPCVD of oxide.

Space module

Dry etch step

The key element of a dry etch is that **it is anisotropic:**

the nitride is etched much faster in the vertical direction than in the lateral direction.

Stopped once the TEOS oxide layer is reached

Detecting when the TEOS oxide is reached during dry etch is relatively easy because TEOS oxide and nitride are very different materials

When the TEOS oxide is reached, there is still nitride present next to the gate!!!

Second advantage:

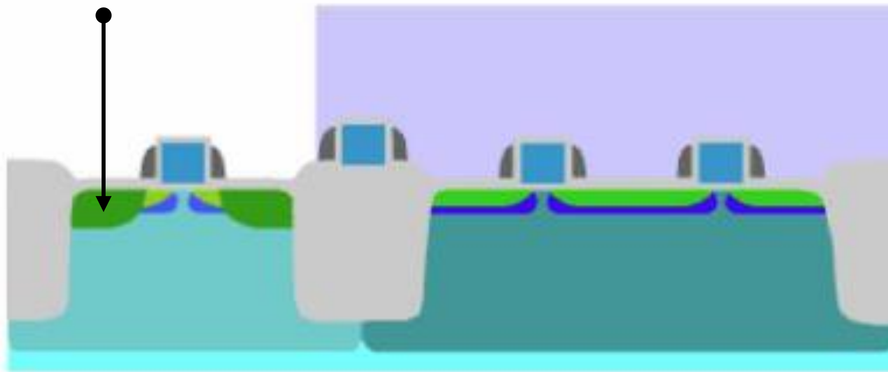
thanks to the TEOS Dry etch oxide, the silicon beneath is not damaged and thus no re-oxidation has to be done!

Third advantage

since this **dry etch step is selective to oxide**, **the field regions are not damaged**

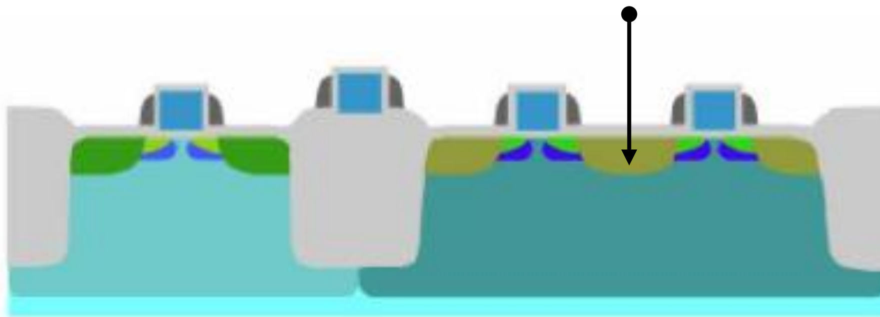
Junction module

n- type implantation
Arsenic, phosphor



Resist strip
Oven anneal

p- type implantation
Boron



Resist strip
Rapid Thermal Process

Junction module

Step 1**: Litho Step**

Step 2**: implant NMOS**

With the photo resist in place, the n- type implantation is done using an **ion implanter**

The ion implanter shoots the dopants into the wafer.

Both **arsenic and phosphor** are n- type elements and can both be used, depending on the transistor optimization.

The dopants are stopped in the thick field oxides and in the spacers.

The spacers create an offset between the gate edge and the source/drain regions.

The dopants are also implanted in the polysilicon gate electrode of the nMOS transistors.

Step 3**: Resist Strip**

Junction module

Step 4**: Anneal (oven) to activate the dopants**

Because the ion implanter shoot the dopants into the wafer, **the dopants will occupy random spaces** between the silicon atoms in the lattice.

However, **to become electrically active the dopants have to become part of the lattice**, replacing silicon atoms.

The same sequence for p-MOSFETs, junction implant is used.

The p-dopants (boron) are implanted using the ion implanter.

Again, some dopants are stopped in the photo resist, in the field oxides and also in the polysilicon gate electrode of the pMOS transistors.

After the resist strip heating is done for a very short time with an RTP - Rapid Thermal *Processing - step* .

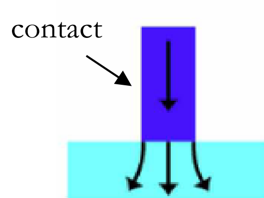
An oven anneal would cause problems: p type dopants are very small (certainly compared to n-type dopants) and therefore diffuse easily, especially when heated.

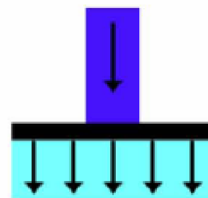
Salicide module

SALICIDE = Self-Aligned Silicides

- Silicide has to be self-aligned to gate and S/D area
- no silicide growth on spacers and isolation regions (= short circuits)

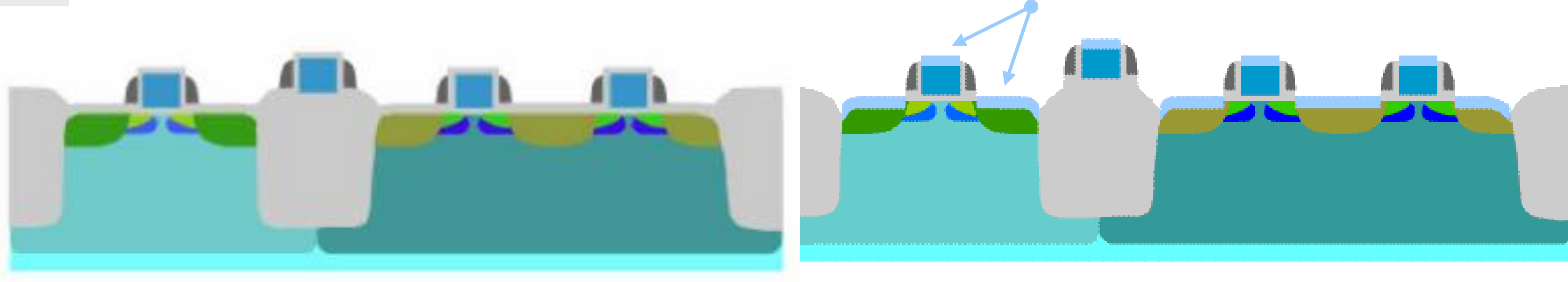
The silicide module serves as a means to lower source/drain/gate resistance





Silicide also avoid current crowding

Silicide on the source, drain and gate



Why Salicide?

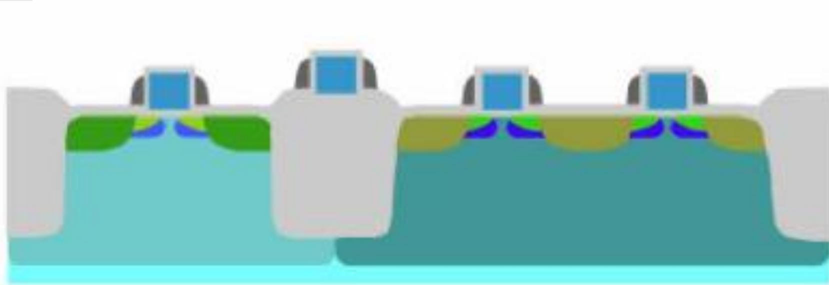
Silicides **lower the contact resistance** between the transistor and the contacts implemented in the BEOL.

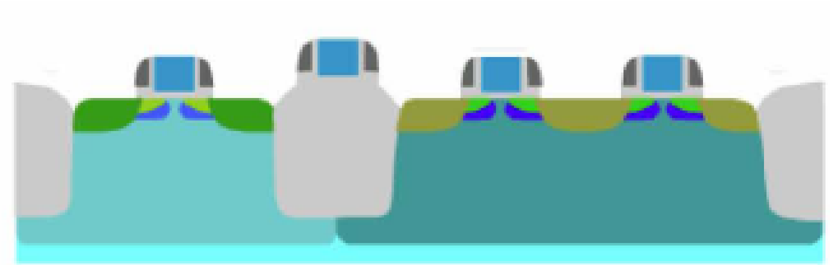
The salicide stands for self aligned silicide: the silicide is formed at the gate source and drain areas at the same time and does not require any litho step.

A silicide is an allow of silicon and a metal (Ti, Co, Ni..) obtained by a high temperature step.

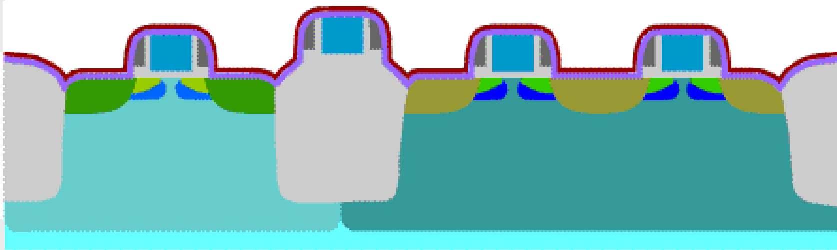
The silicide has a much lower resistivity then the doped silicon (typically a few Ω/sq)

Salicide module

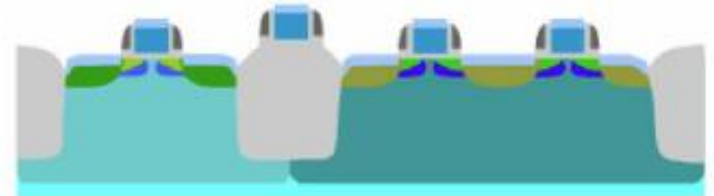




Wet Etch (HF)= Removal of oxide on top of gate, source and drain area



Metal (Co or Ni) is sputtered



Rapid thermal process (RTP1) to allow the reaction metal silicon and selective etch to remove the un-reacted metal

Salicide module

Fabrication steps:

First of all **a HF (hydrofluoric) dip** is done to remove the damaged oxide above the source/drain regions.

It is unavoidable that also a small part of the field oxide is removed.

It is especially a serious problem if too much of the spacers is removed because this can result in bridging.

Nitride spacers do not have this problem and this is one of the reasons why they are used nowadays for small dimensions.

After the oxide is removed, a metal is sputtered onto the wafer surface.

In older technology nodes (before 250 nm) this was usually **titanium and cobalt (130nm).**

For current technology nodes, **nickel** gives better results.

The metal will - in a later process step - react with the silicon beneath, resulting in nickel silicides.

Salicide module

RTP 1

Bridging effect. After sputtering, a first rapid thermal processing (RTP) step is required.

Due to the heat, **a chemical reaction will occur between the first sputtered metal layer and the silicon beneath**.

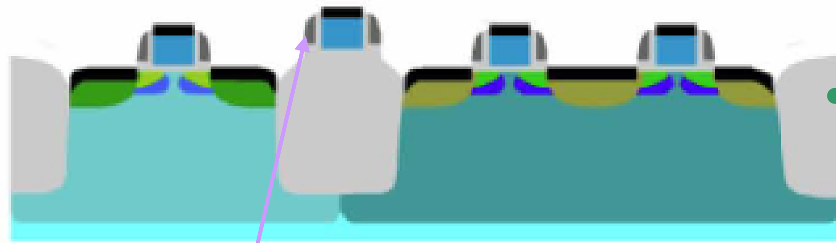
If there is too much heating, the silicided regions will grow into each other. **They will bridge.**

Wet etch

Now both the un-reacted metal and the cap can be removed using a wet etch.

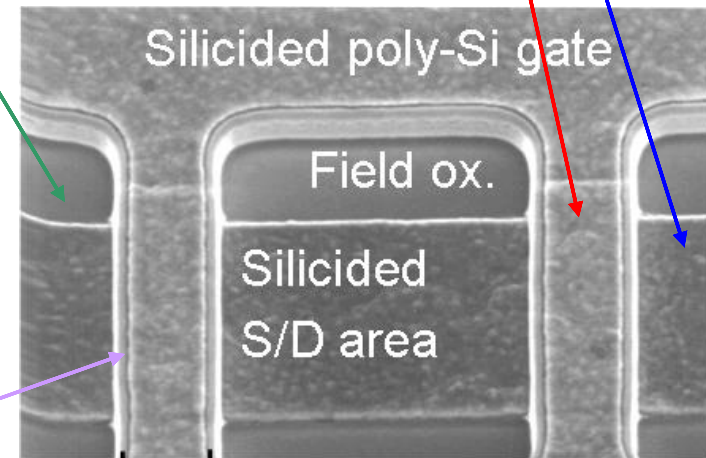
A dry etch is necessary when the etching has to go in only one direction. But in this case, etching has to happen in all directions. Therefore this is a wet etch.

Salicide module



Rapid thermal process (RTP2)

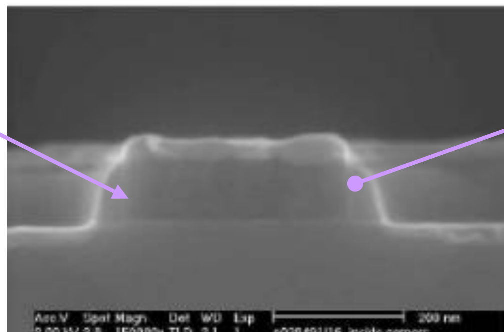
Top view



Sidewall spacers

Cross section

Spacer



Salicide module

RTP2

In order to avoid bridging, the duration of the RTP 1 step was limited. However, as a result, the structure of the silicides is far from optimal.

Therefore a second RTP treatment, called **RTP2, is done when the silicide region are far apart after the selective etch.**

The RTP2 step **improves the conductance** of the silicided regions significantly.

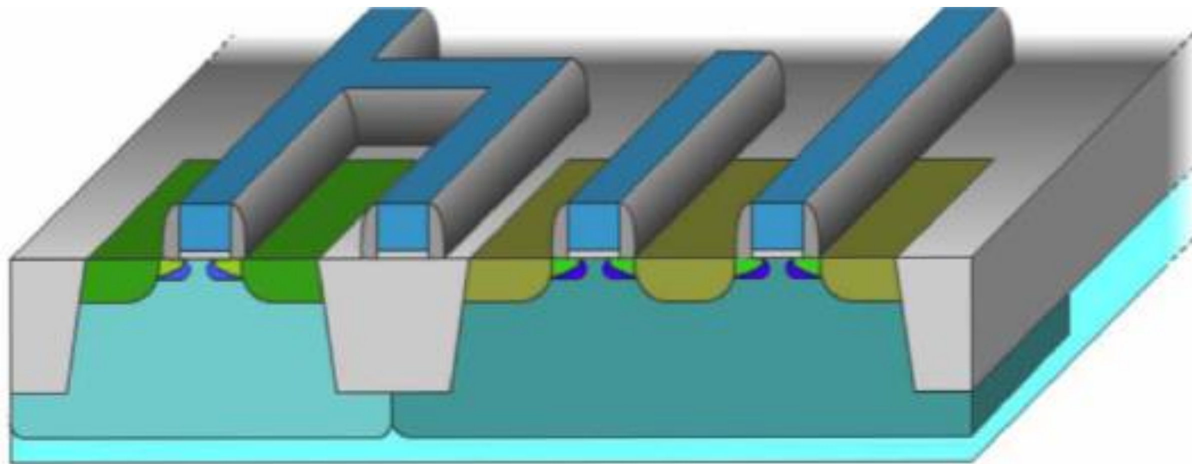
Salicide module

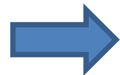
Summary

- Silicides are implemented for various reasons.
- The most important one being a decrease in resistance.
- Several materials have been used to create these silicides. Nowadays cobalt silicides are the most common.
- An important phenomenon that can occur is bridging.
- Implementing 2 heating steps instead of one avoids this.

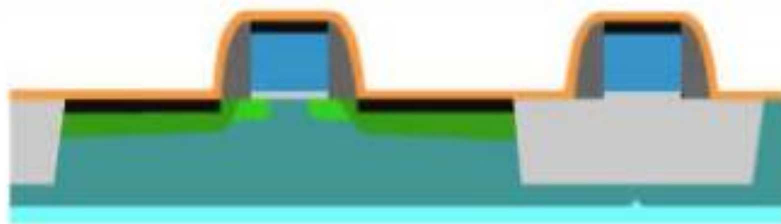
FEOL - the end

Front end of Line

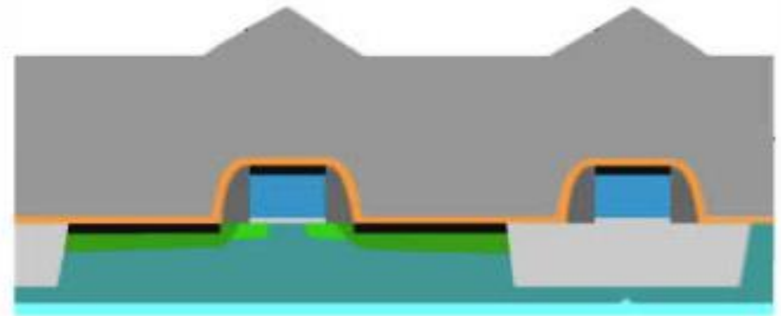


Next step  **Back end of line**

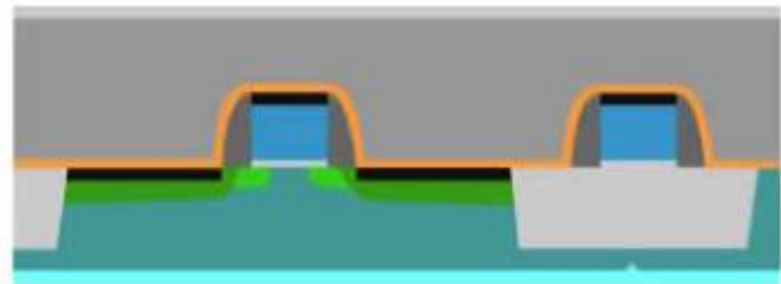
The Pre Metal Dielectric module (PMD) or Inter Level Dielectric (ILD) module



PMD liner

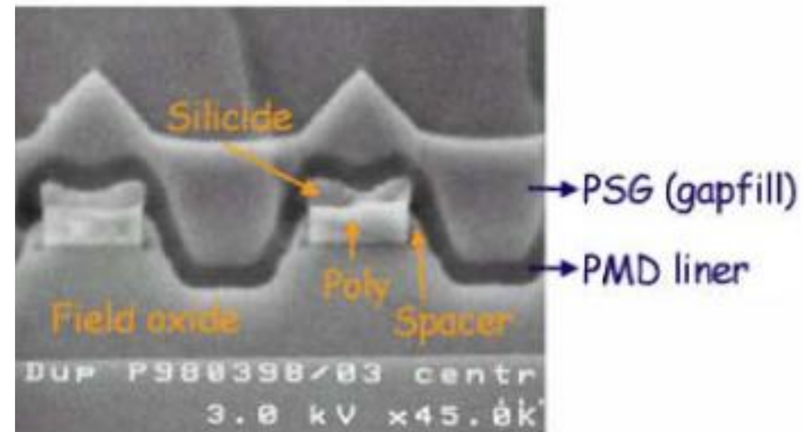


PSG



oxide

Step 1: PMD Liner
Step 2: Gaps filling PSG
Step 3: Polishing (CMP)
Step 4: Oxide Deposition



Pre-metal dielectric module for BEOL

PMD module Overview

called also Inter Level Dielectric (ILD) module, creates the first dielectric between the silicide and the metallization.

Step 1. Deposition of the PMD liner

The first step of the IMD module is the deposition of the PMD liner. The PMD liner is a thin silicon dioxynitred (SiON) layer.

This SiON liner has three functions:

- ❑ The SiON liner protect the transistor from being damaged by the next step.
- ❑ The SiON liner can also be used as an etch Stop layer during the contact etch
- ❑ The SiON liner is also used as an Anti- Reflective Coating (ARC for the contact Lithography (contact critical dimension).
- ❑ The SiON liner is also used is most advanced technology to introduce strain into the device to boost the mobility (tensile for nMOS or compressive for pMOS)

Pre-metal dielectric module for BEOL

After the deposition of the PMD liner the gaps between the poly lines are filled with Phosphor-Silicate Glass (**PSG**).

The PSG is a phosphorous (P) doped oxide. The phosphor immobilizes mobile ions that could eventually damage the Front-End devices.

The triangular shape of the PSG deposition is typical for High Deposition Pressure deposition.It is therefore planarized using CMP.

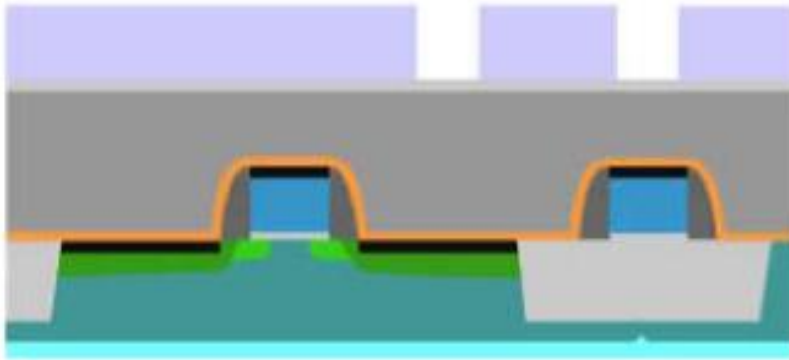
Step 4. PECVD deposition of oxide.

Plasma Enhanced Chemical Vapor Deposition (PECVD) of a thin oxide layer on the PSG layer. (oxide in light grey in the figures and the PSG in dark grey).

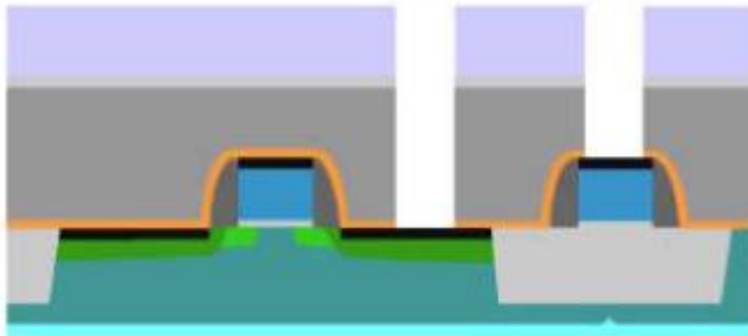
This oxide layer is done to voids resist footing of the contact photo. Footing means that the photo-resist pattern is not accurate near the bottom of the photo resist.

Contact module for BEOL

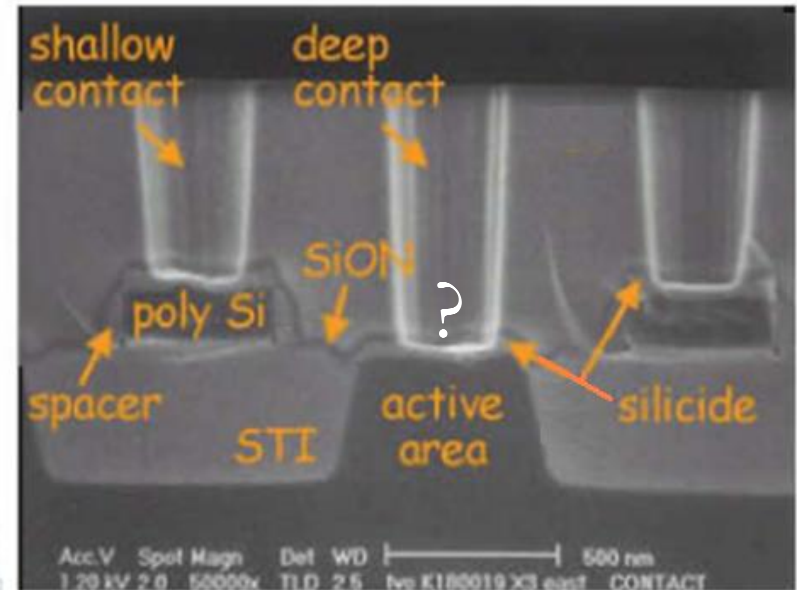
Contact module for Copper back end of line process flow



Contact lithography



Contact hole etch



Contacts are made of Tungsten

Contact module for BEOL

Step 1. A lithography step.

The goal is to etch holes in the dielectric (Phosphor-Silicate Glass / PSG layer) that was deposited during the PMD module. Lithography define the pattern to be etched.

Step 2. Contact etch.

After the lithography there is an etch step. In the contact etch step holes are formed in the PSG as defined by lithography.

It is important that the etching stops at the silicide (black layer in the figure), otherwise the transistor is damaged. Therefore the etching has to be highly selective toward the silicide.

Contact module for BEOL

There are two different types of contacts:

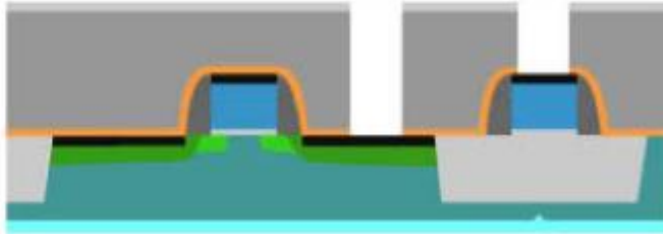
• The deep contact holes. They reach the source and drain of the transistor.

• The shallow contact holes. They reach the poly lines and the gates of the transistors

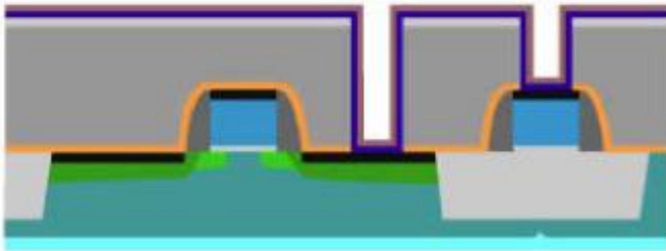
Step 3. remove the Resist by Photo Resist Strip

The cross section gives you a good overview of the previous FEOL and these initial BEOL process modules. From the FEOL , the active area, STI, Spacer, Poly Si, and silicide are visible with the SiON layer on top.

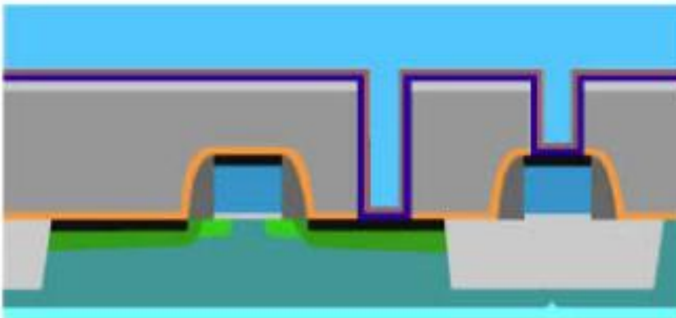
Contact hole module for BEOL



After contact hole resist Strip



Contact hole clean and adhesion barrier deposition



Tungsten (W) deposition

Contact hole module for BEOL

First the holes are cleaned by a soft etch and then a barrier layer is deposited.

This Ti/TiN barrier is necessary because tungsten has poor adhesion properties to hard oxide.

The Ti layer lowers the contact resistance and has good adhesion properties. The TiN is the barrier that prevents reaction of Si or Ti with the tungsten metal precursors(WF6).

Another property of TiN is that it forms a diffusion barrier for copper.

The Ti/TiN layer is deposited by ionized physical vapor deposition.

Contact hole module for BEOL

After depositing the Ti/TiN barrier the contact needs to be filled with tungsten.

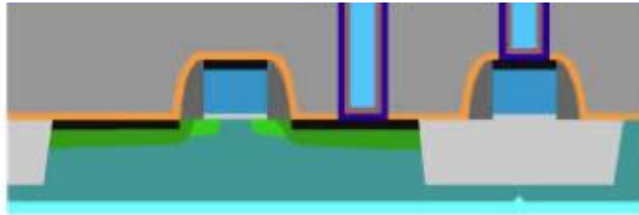
The deposition process must have good step coverage and high deposition rate.

The deposited tungsten (W) should have fine grains and high thickness uniformity.

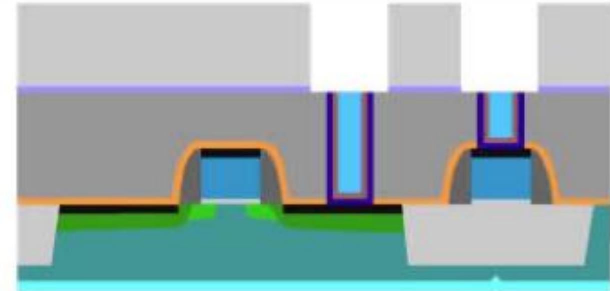
To fulfill these requirements the filling is done in 2 steps :

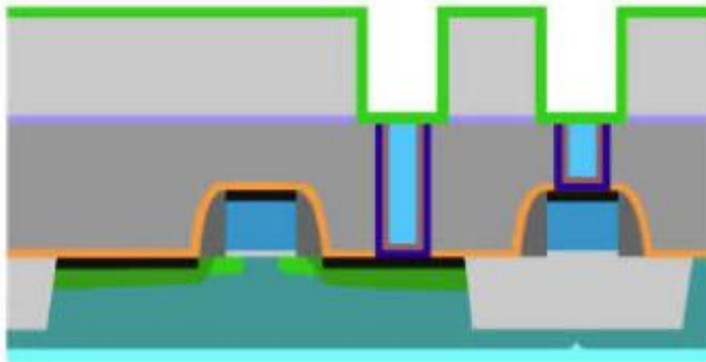
- ❑ First a nucleation layer is deposited followed by a bulk layer.
- ❑ Then, a Planarization is performed by polishing the metal (metal CMP).

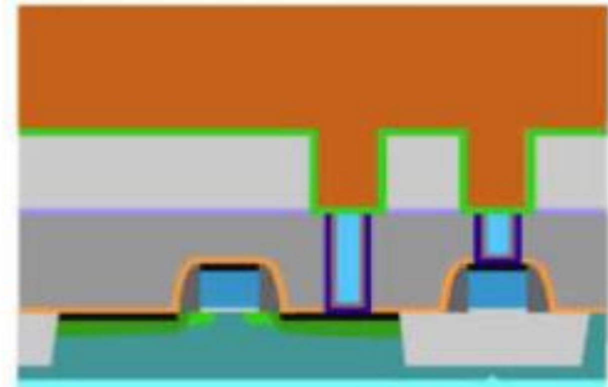
Contact hole module for BEOL



Metal CMP







Contact hole module for BEOL

Tungsten is a metal and shorts all the contacts so it should be removed from the area where it is not needed by metal CMP.

As compared to older technologies in which Al was patterned to implemented the BEOL, modern technologies make use of Cu and damascene approach.

The main reason is the lower resistivity of Cu (~1.7uOhm. cm while ~3 uOhm.cm in case of Al), even for narrow patterns. Moreover, Cu has better electromigration lifetime than Al.

As copper is difficult to etch, the damascene flow is followed, which also requires less steps.

Single Damascene Copper Metal 1 Overview

Prior to the actual copper filling a tantalium nitride / tantalium (Tan/Ta) is deposited. It is a very good diffusion barrier for copper.

(TiN is also a good metal diffusion stopper : Copper atoms could diffuse and damage the transistors)

Copper deposition

Before the trenches are actually filled with copper a thin copper layer called the copper (Cu) seed layer is deposited.

This layer facilitates the deposition of the copper in the next step. Copper is deposited by electro-plating.

The Cu seed layer also improves the adhesion of the copper layer, the grain size and the texture of the copper.

Contact hole module for BEOL

Cu electro plating:

This process require a chemical bath containing copper ions. An electrical field is created between the wafer and an electrode on a different potential.

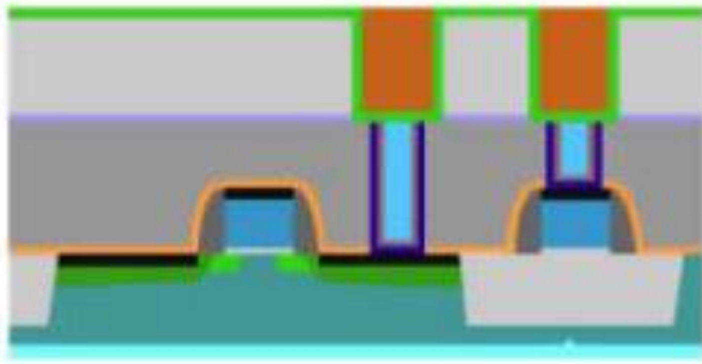
Due to he electrical field the copper ions move towards the wafer. (During Cu electroplating the wafer is connected to a power supply at the edge of the wafer.

If the wafer had a high resistance no Cu seed used) a very large potential would be needed.

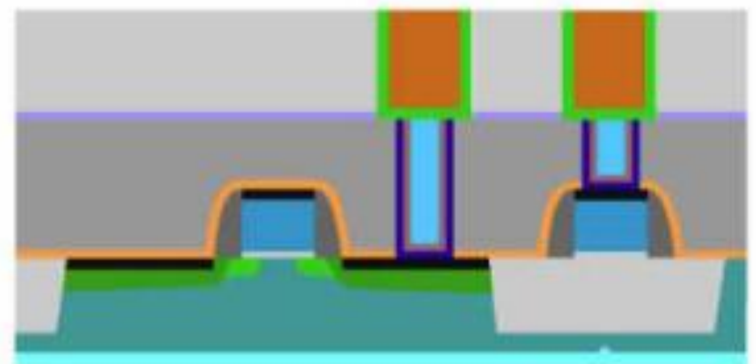
Contact hole module for BEOL

After the electroplating process the wafer is fully covered with copper.

So its has to be removed, in order to isolate the metal lines.



Copper CMP

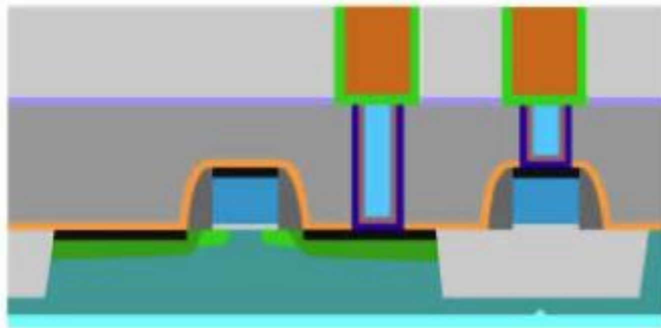


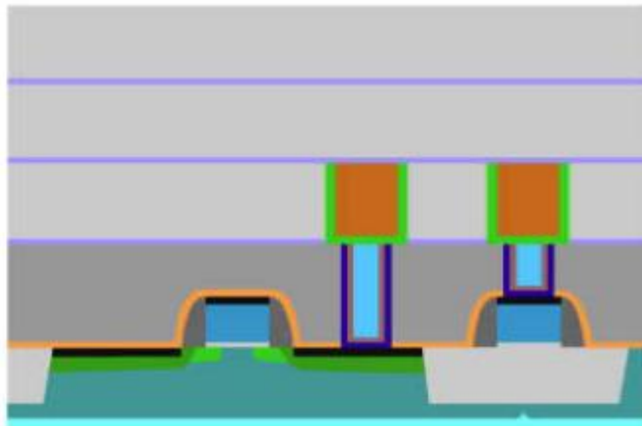
TaN/Ta CMP

Contact hole module for BEOL

After the electroplating process the wafer is fully covered with copper.

So its has to be removed, in order to isolate the metal lines.





Dual damascene ensure that trenches and vias are etched and filled at the same time.

Contact hole module for BEOL

IMD2 layer consists of two oxide lavers with a hard mask in between (also called embedded hardmask)

In the upper oxide layer the trench is etched. The via is etched in the lower oxide layer.

In this way the via connect the trenches of the metal1 layer processed (single damascene) with the trenches that are created in this process module. This is the **metal 2 layer.**

The purple layers in the figure are silicon carbide (SiC) layers.

SiC is used as a dielectric **hardmask**.

A hardmask ensures that an etched trench or via has the correct depth.

Contact hole module for BEOL

The hard mask has also other interesting advantages: it is a good etch stop layer, a good diffusion barrier for copper and also it is an Anti-Reflective Coating (ARC) for lithography.

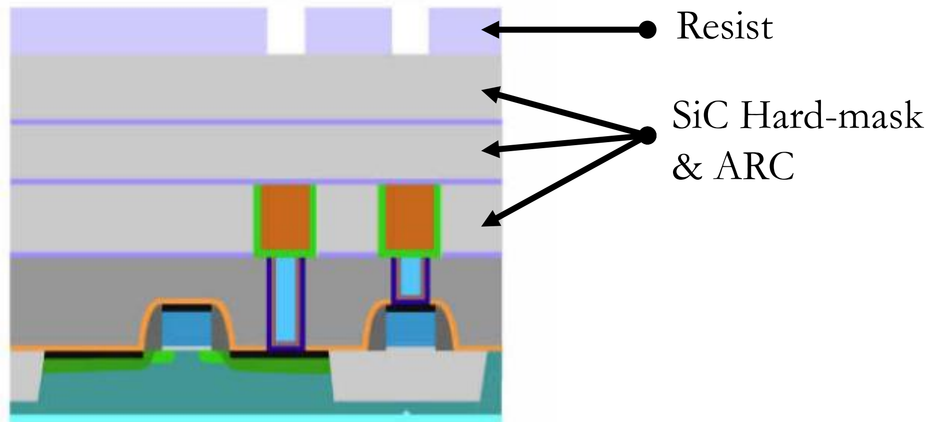
The k value (permitivity) of the dielectric must be small to obtain a **low RC delay**.

The hardmask will also influence the k value of the total IMD layer.

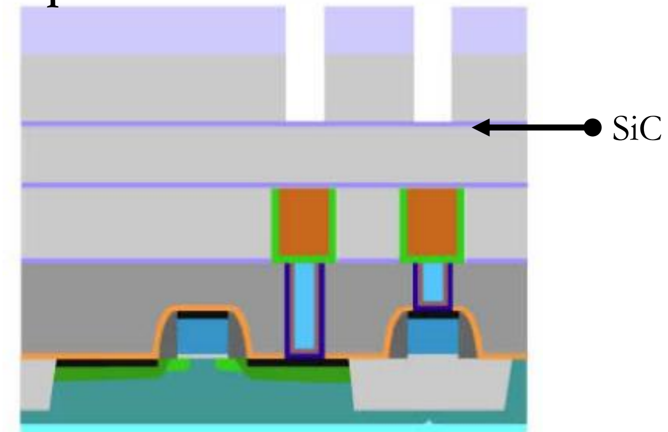
Therefore it is important that the k value of the hardmask is also low.

Contact hole module for BEOL

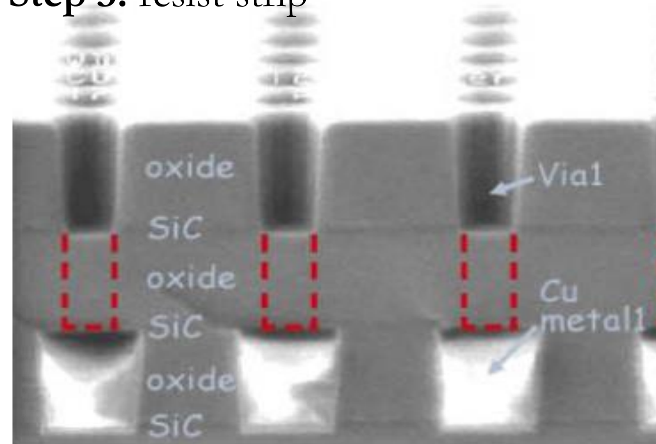
Step 1: Via1 litho



Step 2: Via1 etch



Step 3: resist strip



Contact hole module for BEOL

The patterning module consists of 7 steps:

- ❑ Step 1: Via1 Lithography
- ❑ Step 2: Partial Etching of Via1
- ❑ Step 3: Photo Resist Strip
- ❑ Step 4: Metal2 Lithography
- ❑ Step 5: Underlayer Removal
- ❑ Step 6: Dual Damascene Etching
- ❑ Step 7: Photo Resist Strip

Contact hole module for BEOL

Step 1: Via1 Lithography

The photo resist (light blue) on top of the oxide. The SiC (purple) is an Anti-Reflective Coating (ARC) for lithography. The diameter for the via is fixed to around 0.11 micron for the 90 nm technology.

It might seem strange that via1 is patterned first in the top oxide because the trench should be here while the via should be one level down. This is typical in the "partial via first" damascene approach.

Step 2: Partial Etching of via1

After the definition of the vias by the lithography step, the next step is **etching the vias**.The embedded SiC hard mask acts as the etch stop layer. This step is called **partial** etching because the via is created in the "trench oxide" and it must be one level down in the "via oxide".

Contact hole module for BEOL

Step 3: Photo Resist Strip 1/2

After the lithography and etching step, there is a **photo resist strip**. The photo resist of the lithography of via1 is not needed anymore. It is removed by a dry strip

Step 4: Metal2 Lithography

Now that we patterned the vias, the next step is the trench (Metal2) lithography step.

This is a difficult one because it needs to be done on a surface with severe topography, because the vias are already etched. To solve these difficulties a **bilayer** for the trench lithography can be used. The first layer is also called the **underlayer** (UL), illustrated in dark purple. This layer fills the vias so that the surface is smooth for lithography. This is also referred to as planarization. The second layer is the **imaging layer** (IL). It is deposited on top of the underlayer and it is the photo resist for etching the trenches.

Contact hole module for BEOL

Step 5: Underlayer Removal

After the trenches are defined by the lithography step, the underlayer is not needed anymore. It is removed for the next step, the dual damascene etch.

Step 6: Dual Damascene Etching

Now we reach the last etch step in the patterning module. The picture schematically show the dual damascene etch of the **vias and the trenches**.

It is a difficult module because etching the trenches should stop on the first etch stop layer and etching the vias should stop on the second etch stop layer. The SiC hardmask is removed after etching.

Contact hole module for BEOL

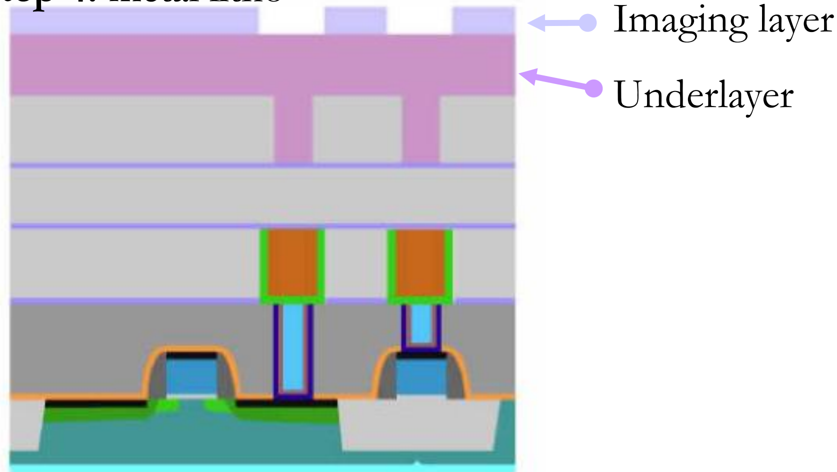
Step 7: Photo Resist Strip

Now you see the patterned IMD layer in real photos. The vias (via1) are etched on top of the metal1 layer (Cu metal1). The metal2 trenches will connect the vias.The bottom picture shows a wafer's top view after patterning the trenches and vias.

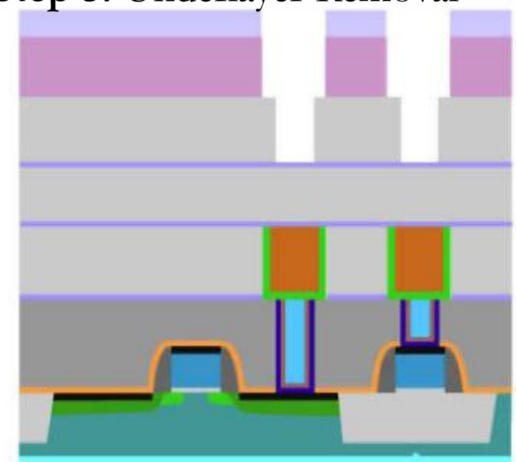
Summary: The IMD layer consists of two hardmask (SiC) and two oxide layers. All layers in the IMD stack influence the total k value.Therefore, the hardmask material should be chosen carefully.The hardmasks act as an Anti-Reflective Coating (ARC) during the lithography steps. The trench lithography requires a planarization of the surface. The surface is rough because vias are already patterned.Then the patterned structures are filled with metal, they will interconnect metal 1 lines.

Contact hole module for BEOL

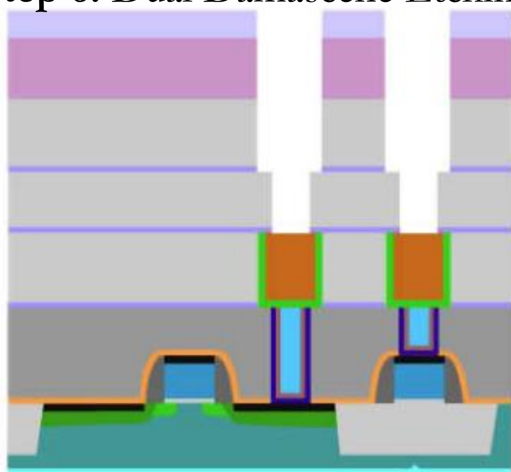
Step 4: metal litho



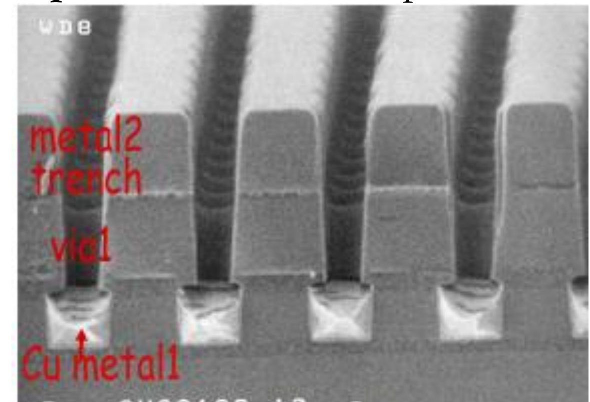
Step 5: Underlayer Removal



Step 6: Dual Damascene Etching



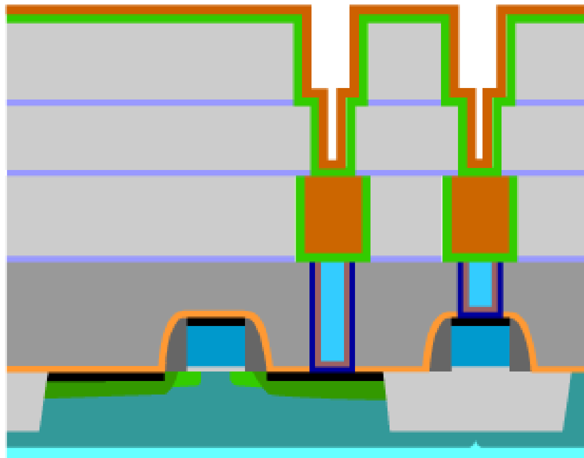
Step 7: Photo Resist Strip



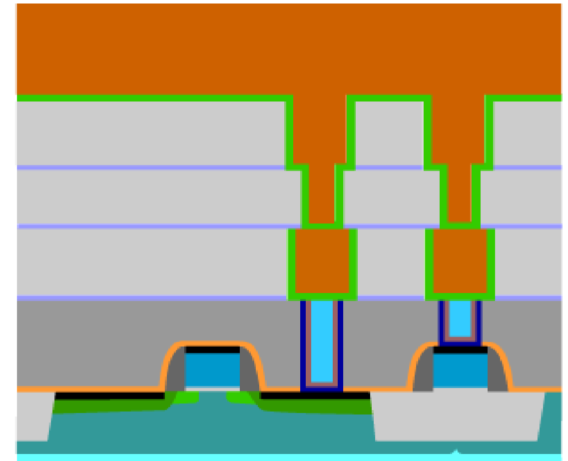
Top view of vias and trenches

Contact hole module for BEOL

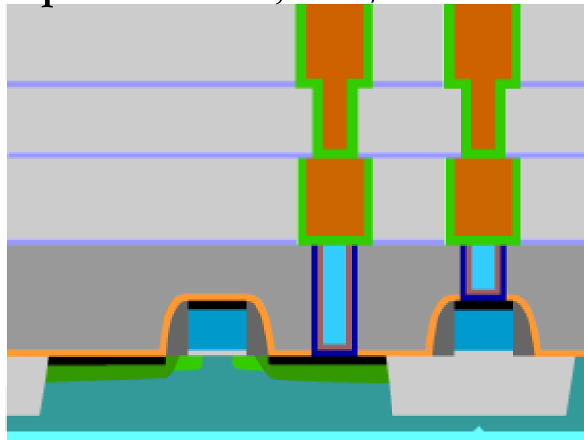
Step 8: Preclean & Deposition of TaN/Ta and Cu seed

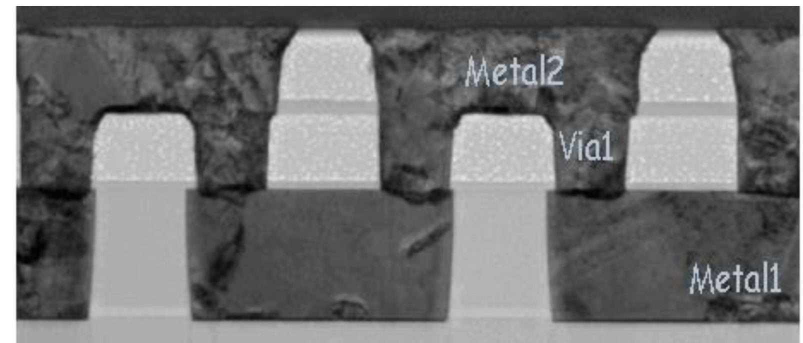


Step 9: Cu electroplating & anneal



Step 10: Cu CMP, TaN/Ta CMP





Contact hole module for BEOL

Dual Damascene Copper Metal2 Module: trench filling

In the copper Metal2 module the patterned vias and trenches are filled with copper. Several steps are required to fill the patterned trenches and vias:

- Step 1: Degas and Argon (Ar) preclean step
- Step 2: Deposition of TaN / Ta
- Step 3: Deposition of Cu seed
- Step 4: Electroplating of copper
- Step 5: Annealing at 250 °C for 30 seconds
- Step 6: Cu CMP
- Step 7: TaN/Ta CMP

Contact hole module for BEOL

Step 1: Preclean step

The trenches and vias are cleaned.

Step 2: Deposition of TaN/Ta

The Tantalum Nitride / Tantalum (TaN / Ta) barrier is deposited to form the diffusion barrier for copper.

Step 3: Deposition of Cu seed

A Cu seed layer required to enable the electroplating process is deposited

Step 4: Electroplating of Copper

The vias and trenches are filled with copper simultaneously. (Note that with the single damascene approach two steps would be required)

Contact hole module for BEOL

Step 5: Annealing at 250 °C for 30 seconds in H2/N2 ambient

The anneal step prevents the structure of the copper changing with time.

Step 6: Cu CMP

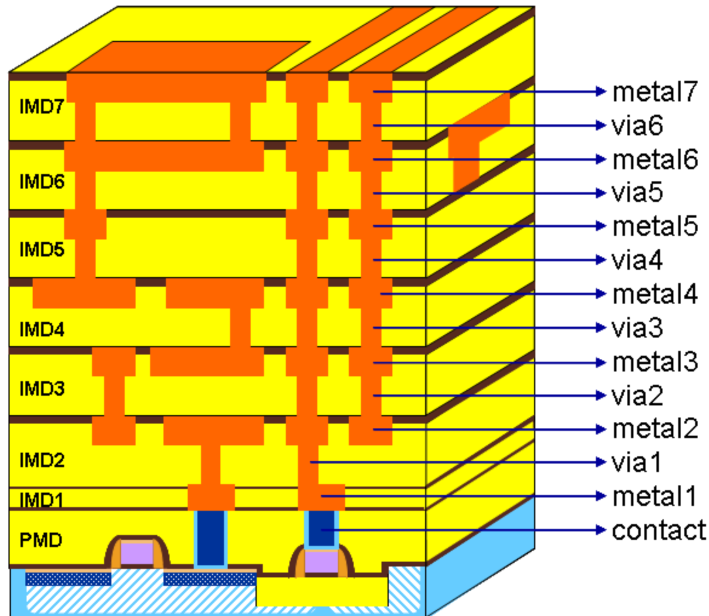
Chemical Mechanical Polishing (CMP) of the Copper, stopping on the TaN/Ta barrier.

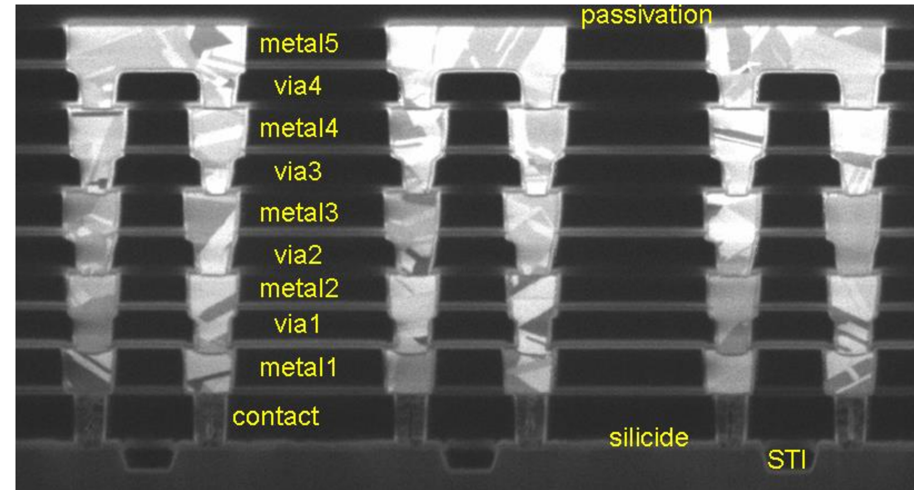
Step 7: TaN/Ta CMP

Chemical Mechanical Polishing of the TaN/Ta barrier. The picture shows a cross-section of the wafer and shows the two metal layers (Metal1 and Metal2) connected with vias (Via1).

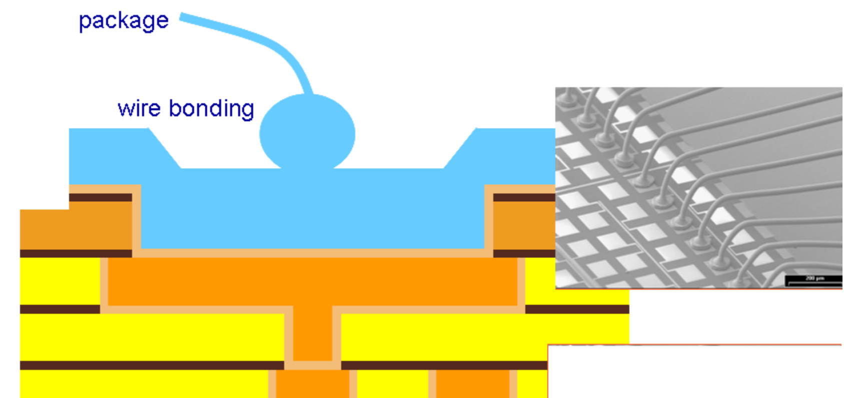
Contact hole module for BEOL

Dual damascene is repeated





Process ends with passivation and packaging



Dual stressor liners – process flow

In recent technology nodes, the traditional gate-oxide-thickness scaling has stalled while device performance improvement was obtained by strain engineering.

A known stress approach to improve both nFET and pFET simultaneously is with the use of dual stress liners respectively with tensile and compressive strain. (use the PMD liner introduced earlier in slide 28)

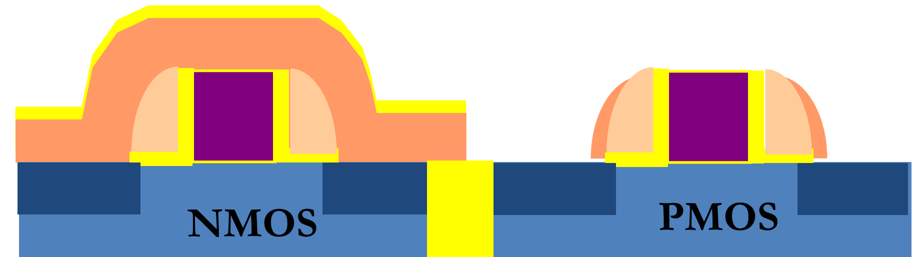
Such approach has been successfully integrated in CMOS flow demonstrating a ring oscillator delay improvement of around 15% over the unstrained reference with 1.5GPa compressive and 0.8GPa tensile 100nm thick SiN films.

Dual stressor liners – process flow

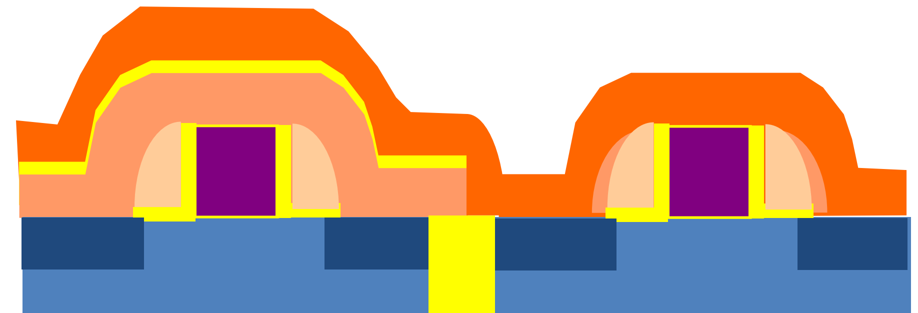
Using the PMD liner (cf slide 33)

- Tensile Nitride Deposition
- Litho Opening pMOS
- Nitride Etch on pMOS
- Strip after etch
- Compressive nitride deposition
- Litho Opening nMOS
- Etch Compressive Nitride
- Strip after etch

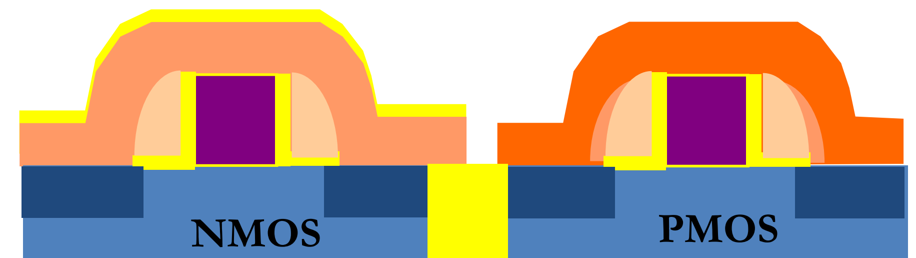
tensile nitride deposition and etch from PMOS



compressive nitride deposition



Removal of compressive nitride from nMOS



FEOL - the end

Deep sub micron effects and parasitics in CMOS

Why should designers care more about "technology details" ?

"FEOL and BEOL technology process, materials and layout dictates the performance limitation. Nanometer design (90nm, 65nm,..) requires designers to be aware of many effects that may be new or just becoming first order.. These effects can't be ignored any longer.. "